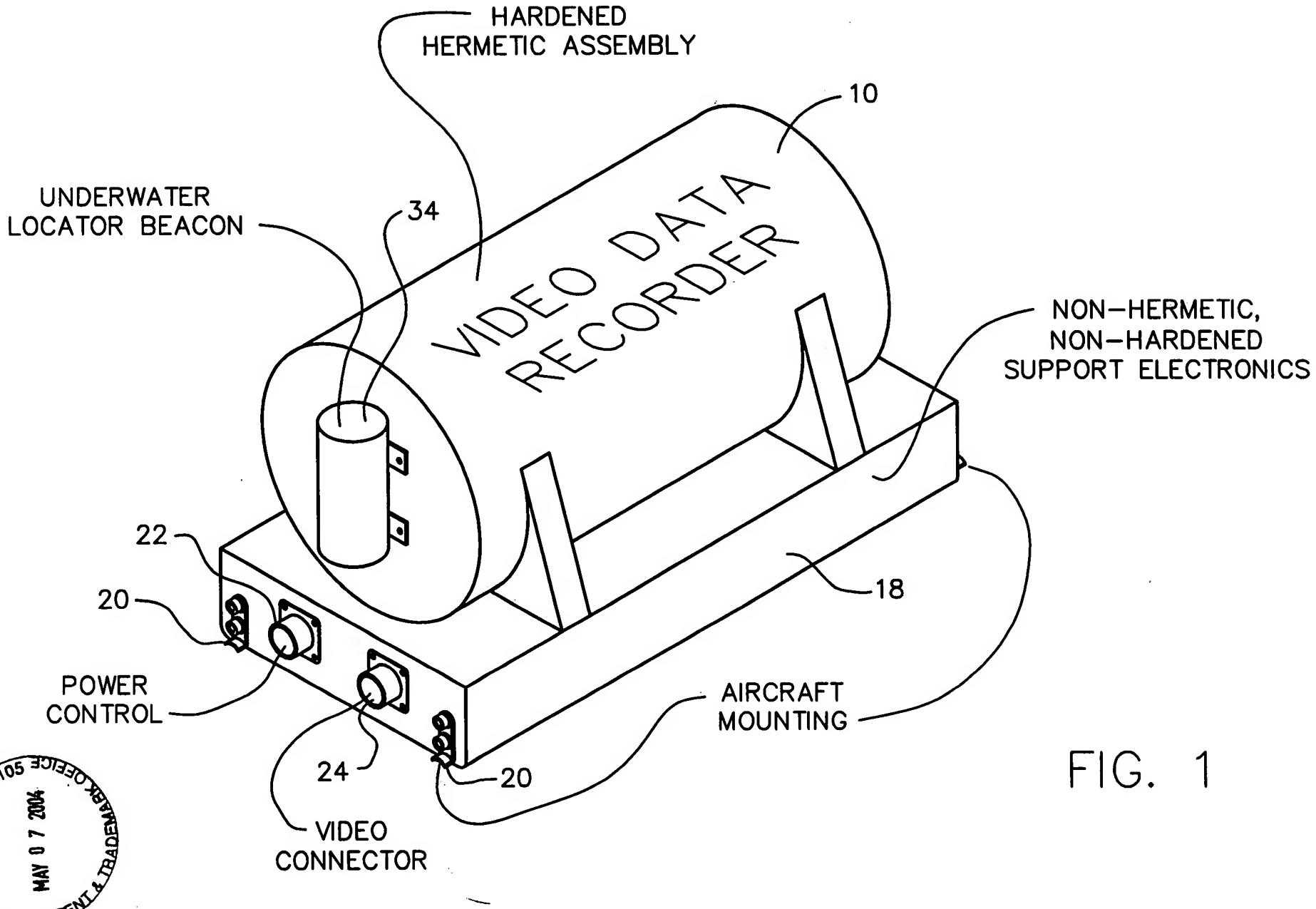

FIG. 1

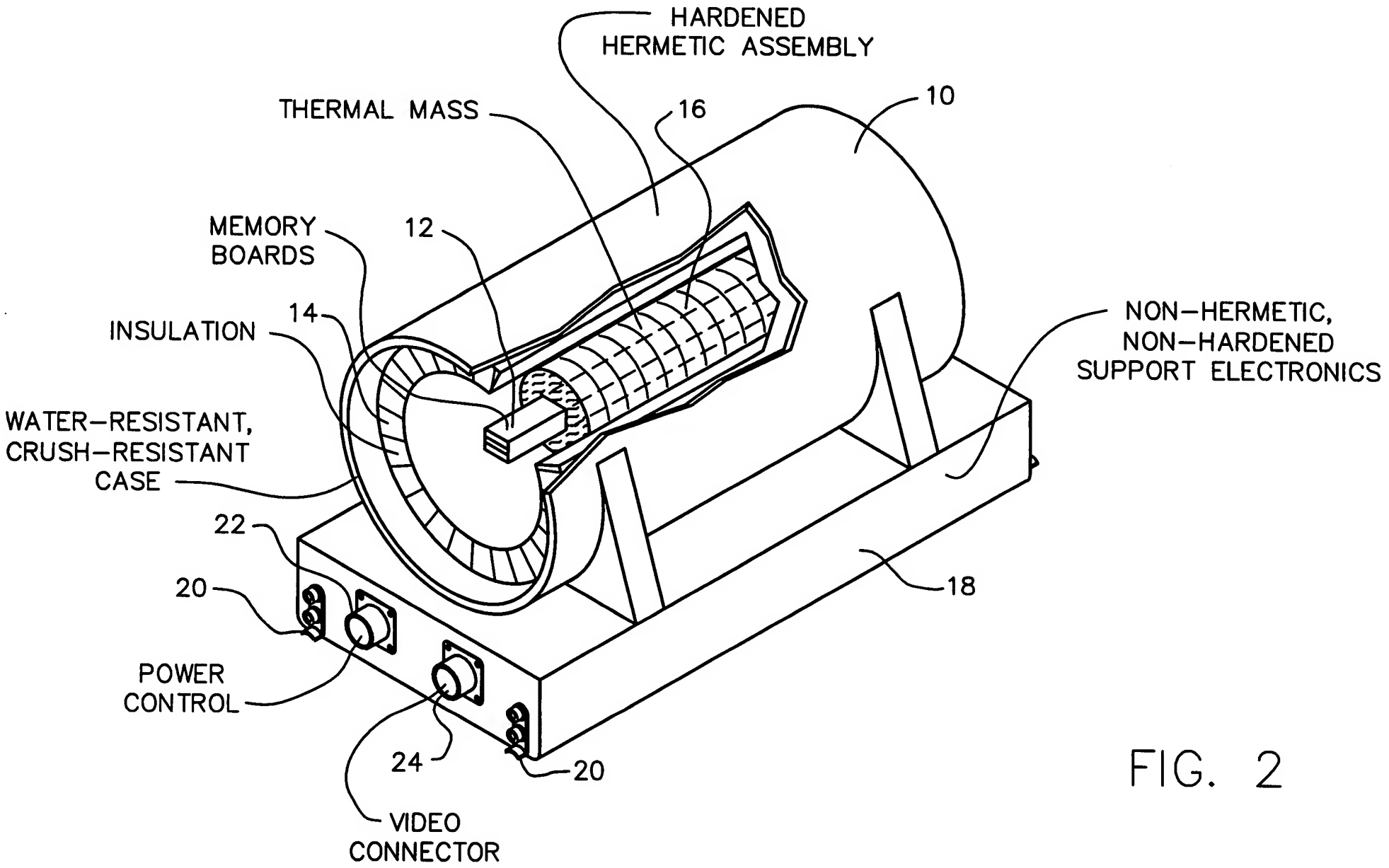
HARDENED
HERMETIC ASSEMBLY
THERMAL MASS
16
10
MEMORY
BOARDS
12
14
INSULATION
NON-HERMETIC,
NON-HARDENED
SUPPORT ELECTRONICS
WATER-RESISTANT,
CRUSH-RESISTANT
CASE
22
20
18
POWER
CONTROL
24
20
VIDEO
CONNECTOR

FIG. 2

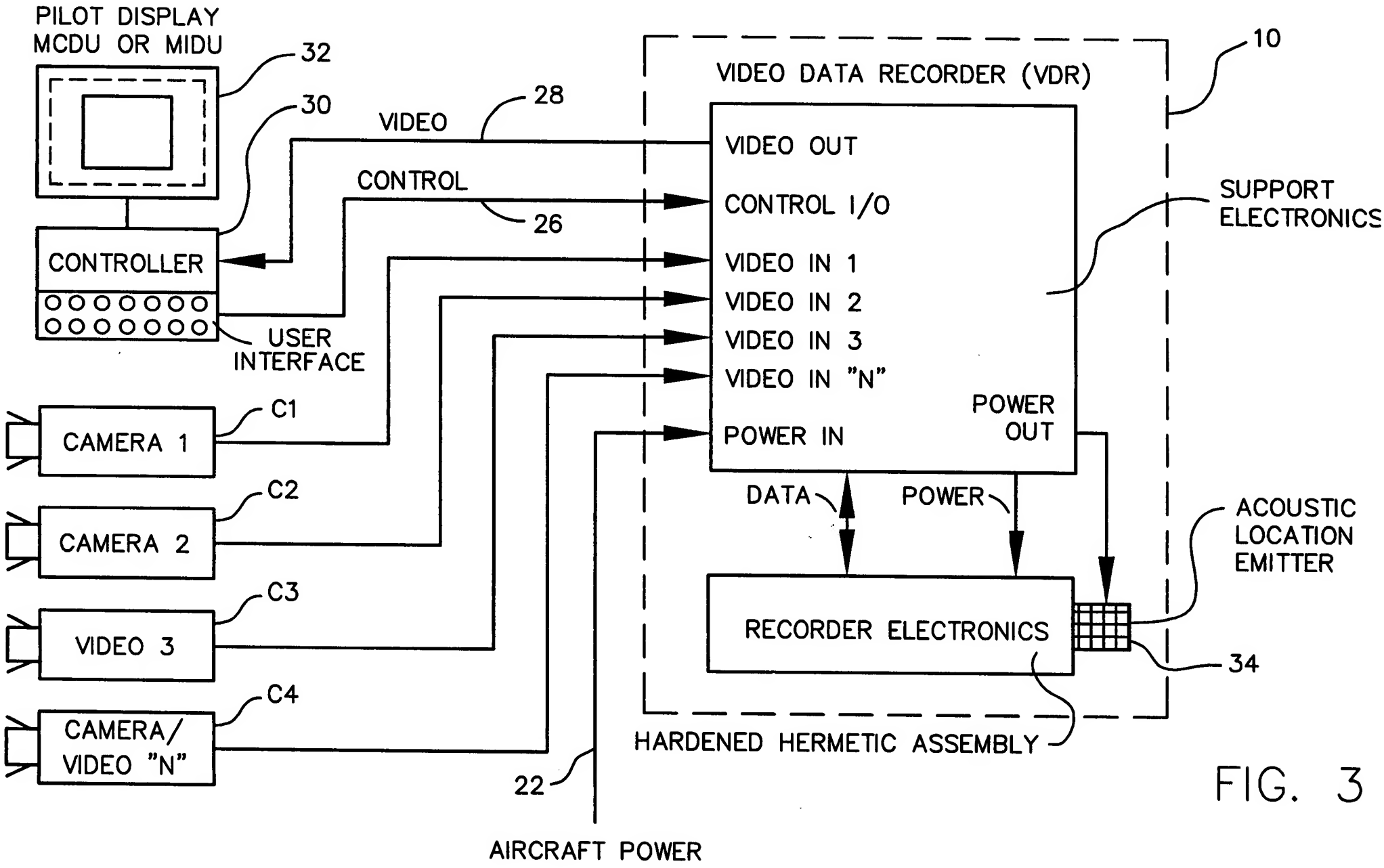
PILOT DISPLAY
MCDU OR MIDU
32
30
VIDEO
28
CONTROL
26
CONTROLLER
USER
INTERFACE
VIDEO DATA RECORDER (VDR)
10
VIDEO OUT
CONTROL I/O
SUPPORT
ELECTRONICS
VIDEO IN 1
VIDEO IN 2
VIDEO IN 3
VIDEO IN "N"
POWER
OUT
POWER IN
C1
CAMERA 1
C2
CAMERA 2
C3
VIDEO 3
C4
CAMERA/
VIDEO "N"
DATA
POWER
ACOUSTIC
LOCATION
EMITTER
RECORDER ELECTRONICS
34
HARDENED HERMETIC ASSEMBLY
22
AIRCRAFT POWER

FIG. 3

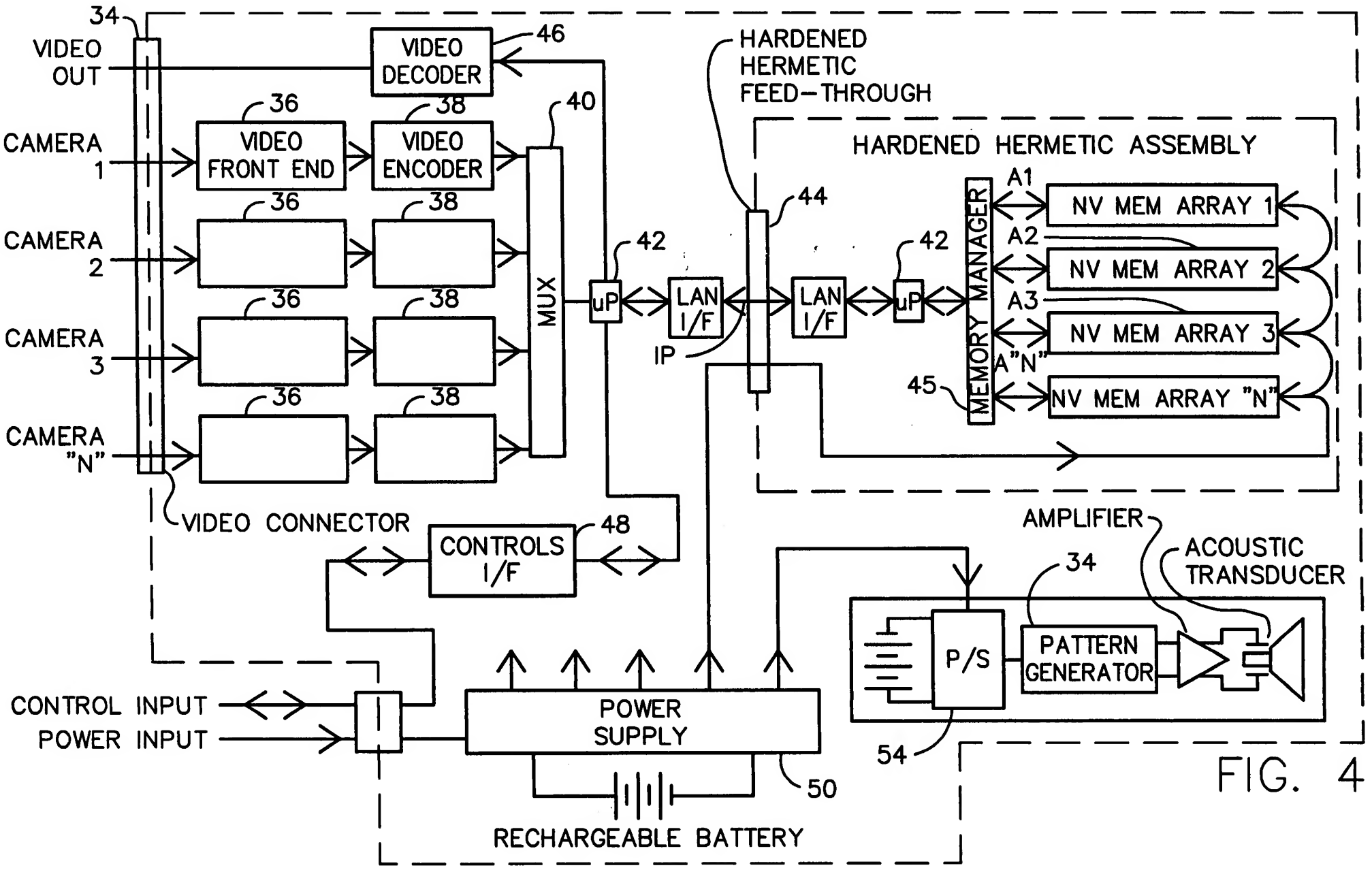
34
VIDEO OUT
VIDEO DECODER
46
HARDENED HERMETIC FEED-THROUGH
HARDENED HERMETIC ASSEMBLY
CAMERA 1
36
VIDEO FRONT END
38
VIDEO ENCODER
40
MUX
CAMERA 2
CAMERA 3
CAMERA "N"
42
uP
LAN I/F
IP
44
LAN I/F
42
uP
MEMORY MANAGER
A1
NV MEM ARRAY 1
A2
NV MEM ARRAY 2
A3
NV MEM ARRAY 3
A"N"
NV MEM ARRAY "N"
45
VIDEO CONNECTOR
CONTROLS I/F
48
AMPLIFIER
ACOUSTIC TRANSDUCER
34
P/S
PATTERN GENERATOR
CONTROL INPUT
POWER INPUT
POWER SUPPLY
50
54
RECHARGEABLE BATTERY

FIG. 4

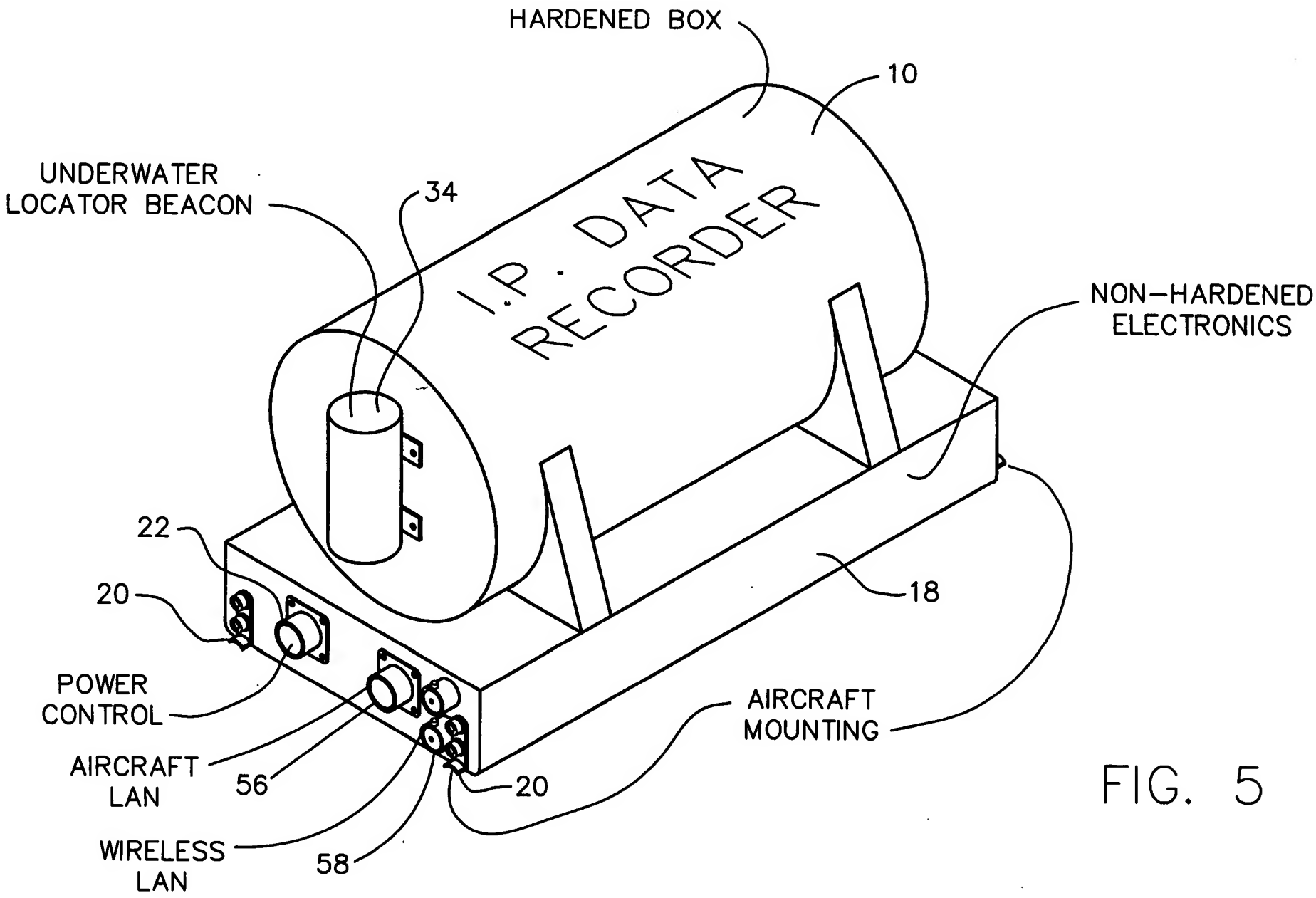
HARDENED BOX
10
UNDERWATER
LOCATOR BEACON
34
I.P. DATA
RECORDER
NON-HARDENED
ELECTRONICS
22
20
18
POWER
CONTROL
AIRCRAFT
LAN
56
AIRCRAFT
MOUNTING
20
WIRELESS
LAN
58

FIG. 5

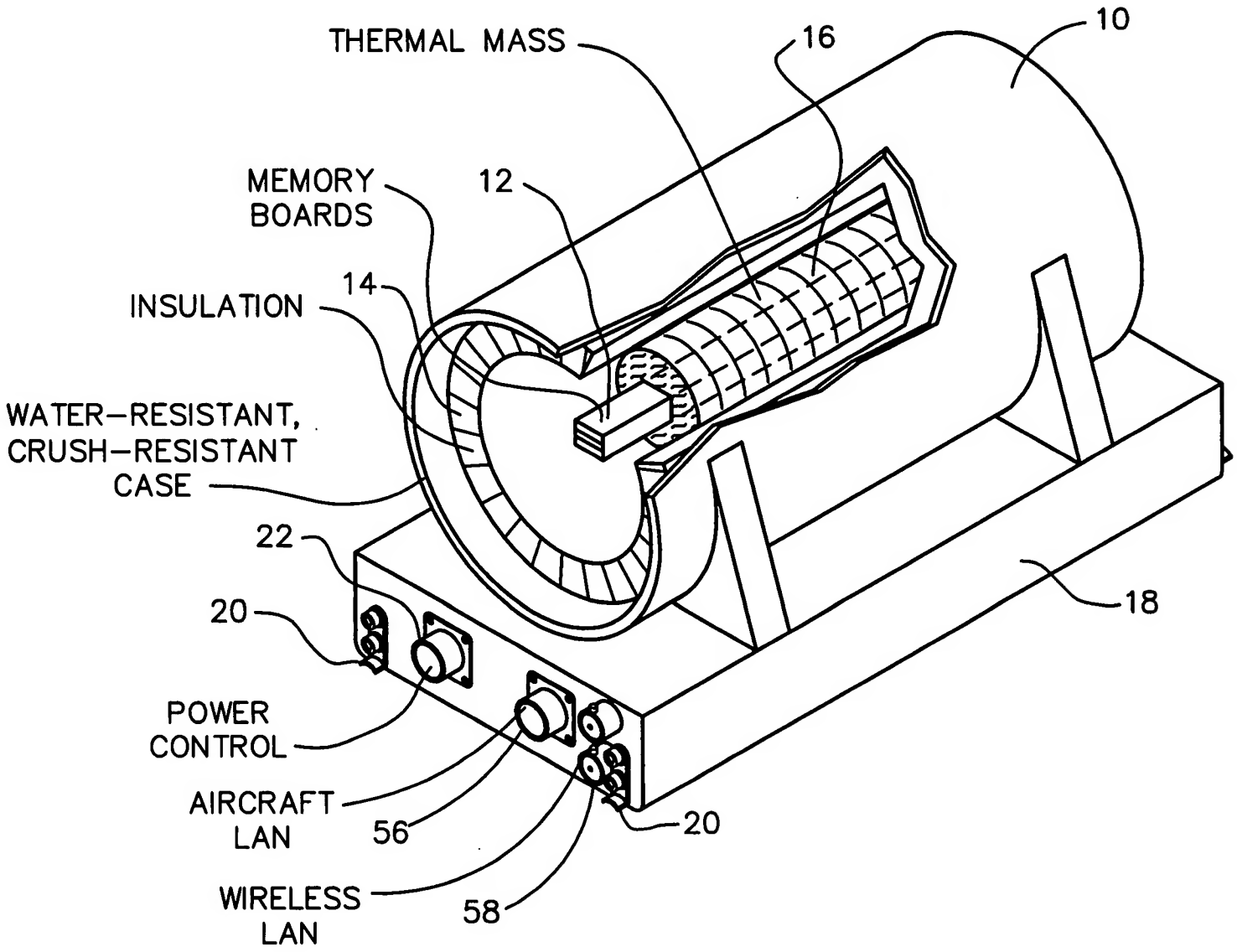
THERMAL MASS
16
10
MEMORY BOARDS
12
14
INSULATION
WATER–RESISTANT, CRUSH–RESISTANT CASE
22
20
18
POWER CONTROL
AIRCRAFT LAN
56
20
WIRELESS LAN
58

FIG. 6

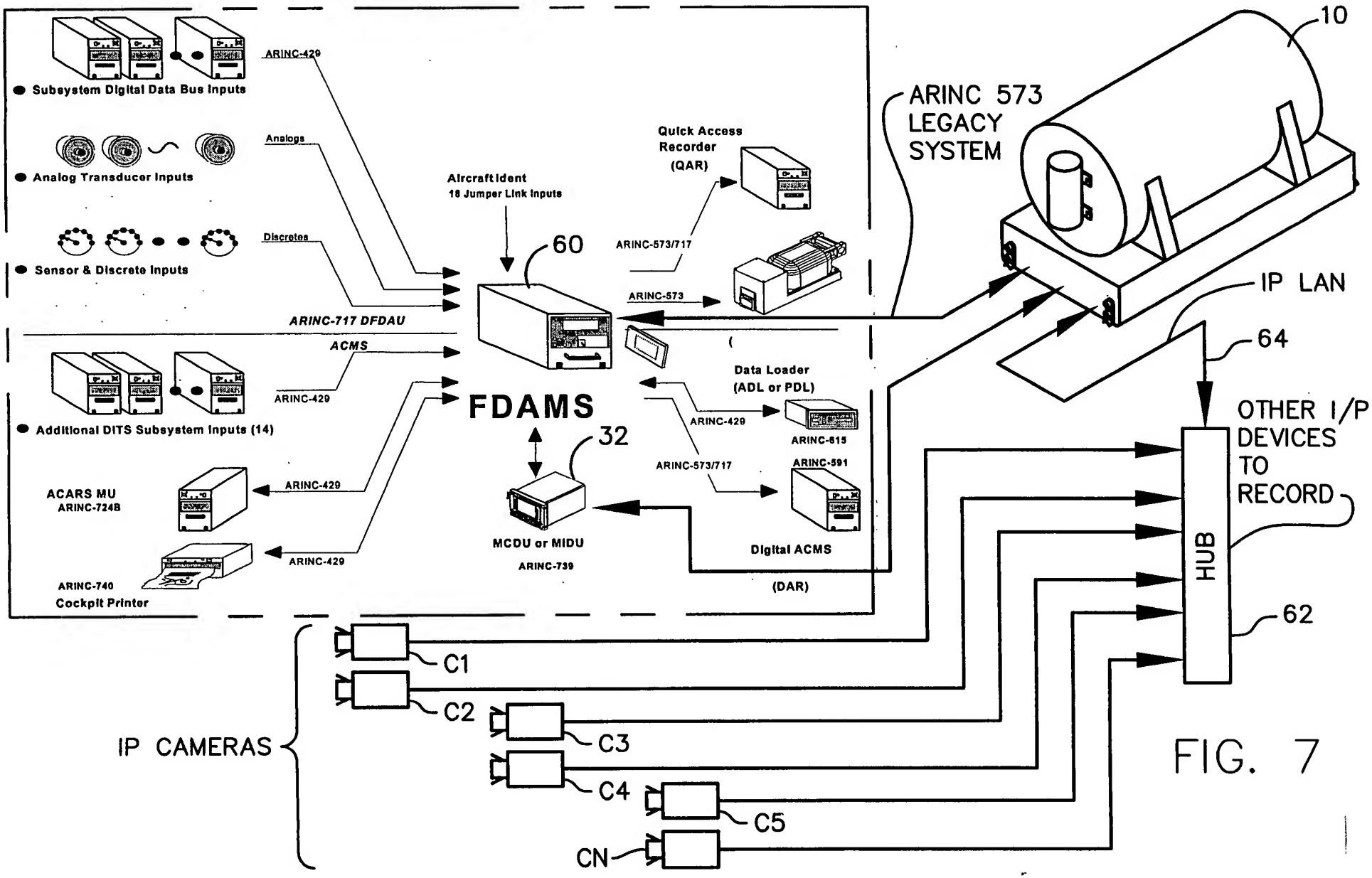
Subsystem Digital Data Bus Inputs
ARINC-429
Analog Transducer Inputs
Analogs
Sensor & Discrete Inputs
Discretes
ARINC-717 DFDAU
ACMS
Additional DITS Subsystem Inputs (14)
ARINC-429
ACARS MU
ARINC-724B
ARINC-429
ARINC-740
Cockpit Printer
ARINC-429
Aircraft Ident
18 Jumper Link Inputs
60
FDAMS
32
MCDU or MIDU
ARINC-739
Quick Access
Recorder
(QAR)
ARINC-573/717
ARINC-573
Data Loader
(ADL or PDL)
ARINC-429
ARINC-615
ARINC-573/717
ARINC-591
Digital ACMS
(DAR)
ARINC 573
LEGACY
SYSTEM
10
IP LAN
64
OTHER I/P
DEVICES
TO
RECORD
HUB
62
IP CAMERAS
C1
C2
C3
C4
C5
CN

FIG. 7

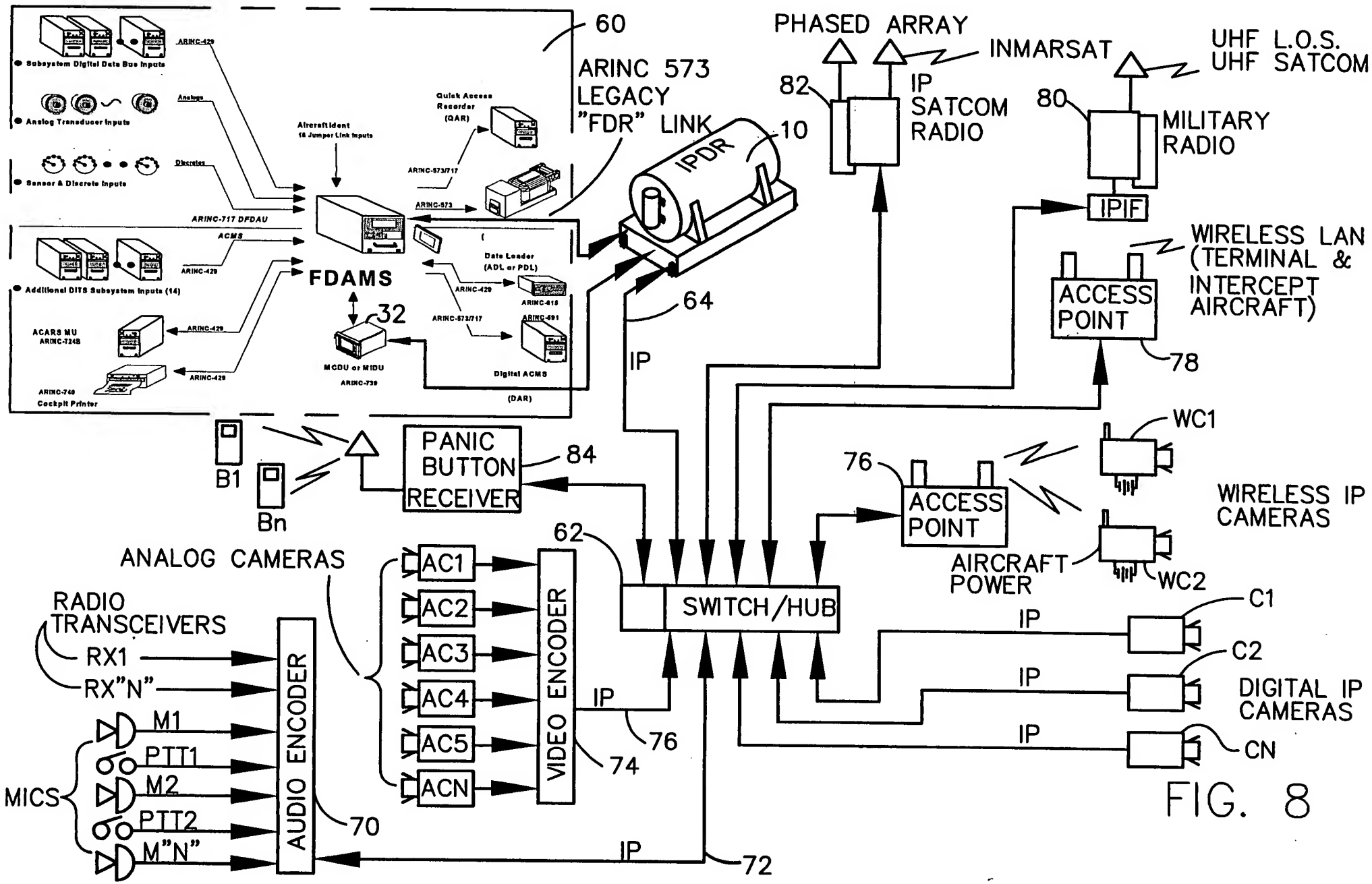
60
ARINC 573
LEGACY
"FDR" LINK
PHASED ARRAY
INMARSAT
UHF L.O.S.
UHF SATCOM
82
IP
SATCOM
RADIO
80
MILITARY
RADIO
IPDR
10
IPIF
WIRELESS LAN
(TERMINAL &
INTERCEPT
AIRCRAFT)
ACCESS
POINT
78
64
IP
FDAMS
32
MCDU or MIDU
ARINC-739
Digital ACMS
(DAR)
Data Loader
(ADL or PDL)
Quick Access
Recorder
(QAR)
Aircraft Ident
16 Jumper Link Inputs
Subsystem Digital Data Bus Inputs
Analog Transducer Inputs
Sensor & Discrete Inputs
Additional DITS Subsystem Inputs (14)
ACARS MU
ARINC-724B
ARINC-740
Cockpit Printer
ARINC-429
ARINC-573/717
ARINC-573
ARINC-717 DFDAU
ACMS
B1
Bn
PANIC
BUTTON
RECEIVER
84
WC1
76
ACCESS
POINT
WIRELESS IP
CAMERAS
AIRCRAFT
POWER
WC2
62
ANALOG CAMERAS
AC1
AC2
AC3
AC4
AC5
ACN
VIDEO ENCODER
SWITCH/HUB
C1
C2
CN
DIGITAL IP
CAMERAS
RADIO
TRANSCEIVERS
RX1
RX"N"
M1
PTT1
M2
PTT2
M"N"
MICS
AUDIO ENCODER
70
74
72

FIG. 8

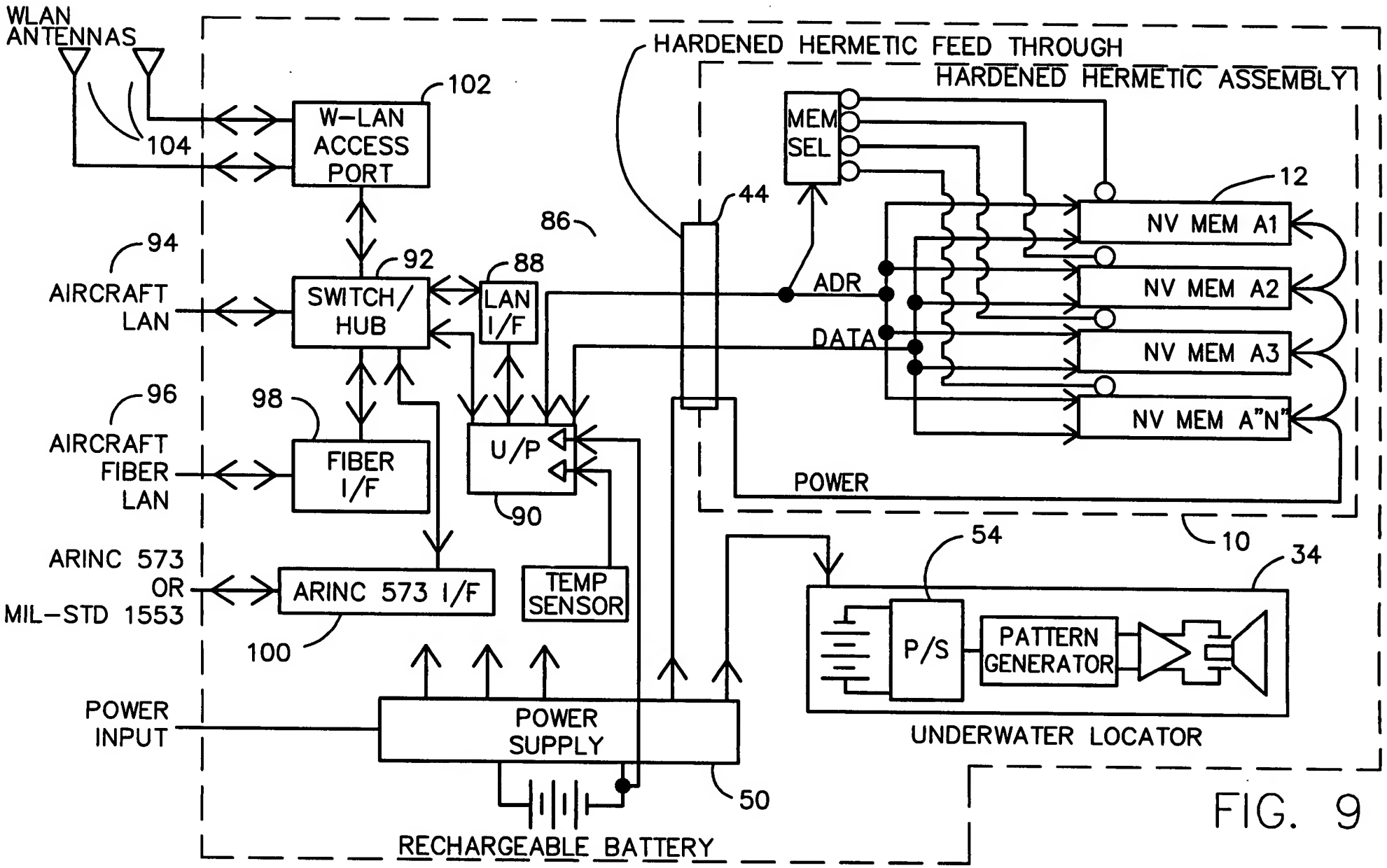
WLAN ANTENNAS
104
W-LAN ACCESS PORT
102
HARDENED HERMETIC FEED THROUGH
HARDENED HERMETIC ASSEMBLY
MEM SEL
12
NV MEM A1
NV MEM A2
NV MEM A3
NV MEM A"N"
44
86
94
AIRCRAFT LAN
SWITCH/ HUB
92
LAN I/F
88
ADR
DATA
96
AIRCRAFT FIBER LAN
98
FIBER I/F
U/P
90
POWER
10
ARINC 573 OR MIL-STD 1553
ARINC 573 I/F
100
TEMP SENSOR
54
34
P/S
PATTERN GENERATOR
UNDERWATER LOCATOR
POWER INPUT
POWER SUPPLY
50
RECHARGEABLE BATTERY

FIG. 9

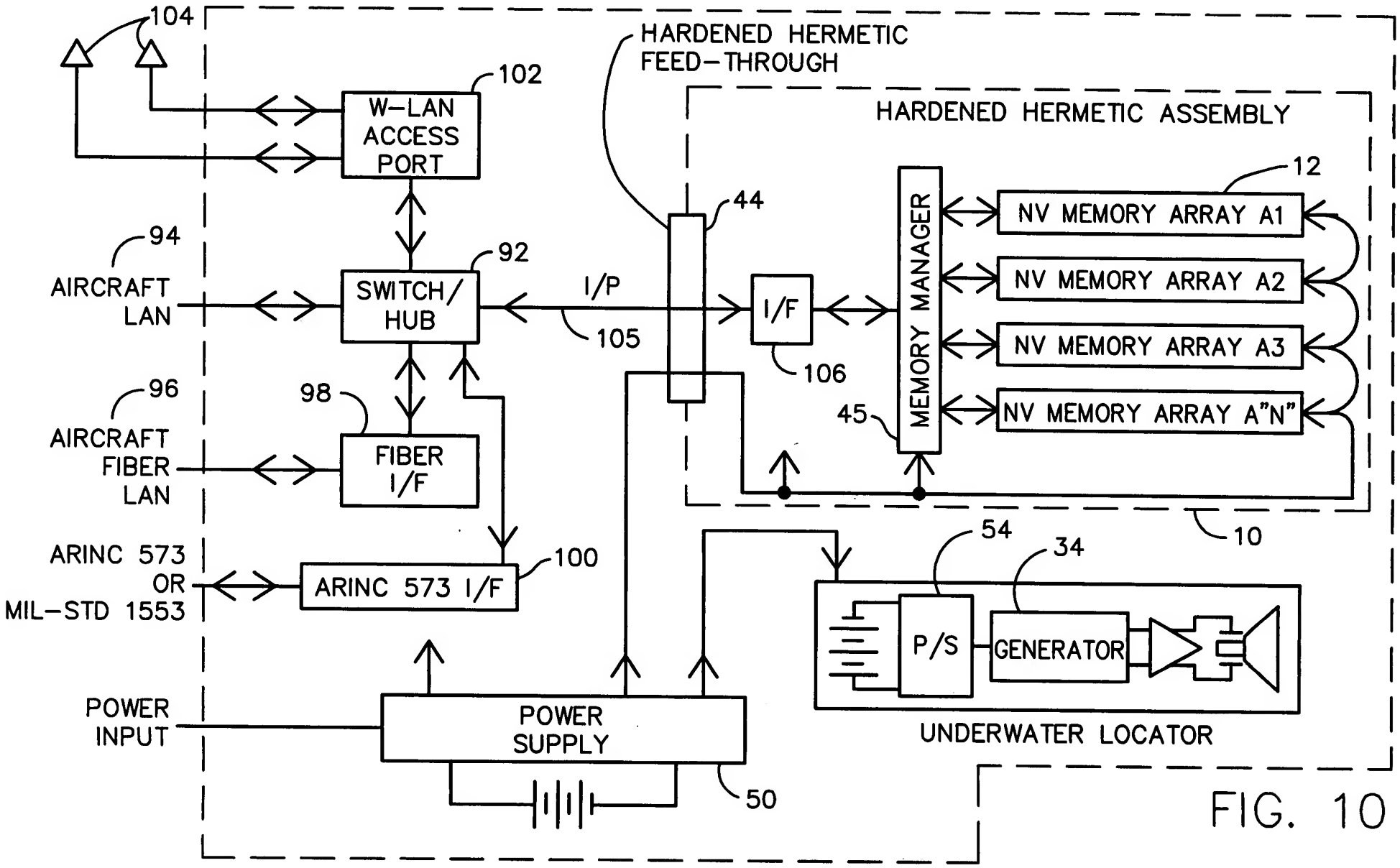
104
HARDENED HERMETIC
FEED-THROUGH
102
W-LAN
ACCESS
PORT
HARDENED HERMETIC ASSEMBLY
12
NV MEMORY ARRAY A1
NV MEMORY ARRAY A2
NV MEMORY ARRAY A3
NV MEMORY ARRAY A"N"
MEMORY MANAGER
45
44
94
AIRCRAFT
LAN
92
SWITCH/
HUB
I/P
105
I/F
106
96
AIRCRAFT
FIBER
LAN
98
FIBER
I/F
ARINC 573
OR
MIL-STD 1553
ARINC 573 I/F
100
10
54
34
P/S
GENERATOR
UNDERWATER LOCATOR
POWER
INPUT
POWER
SUPPLY
50

FIG. 10

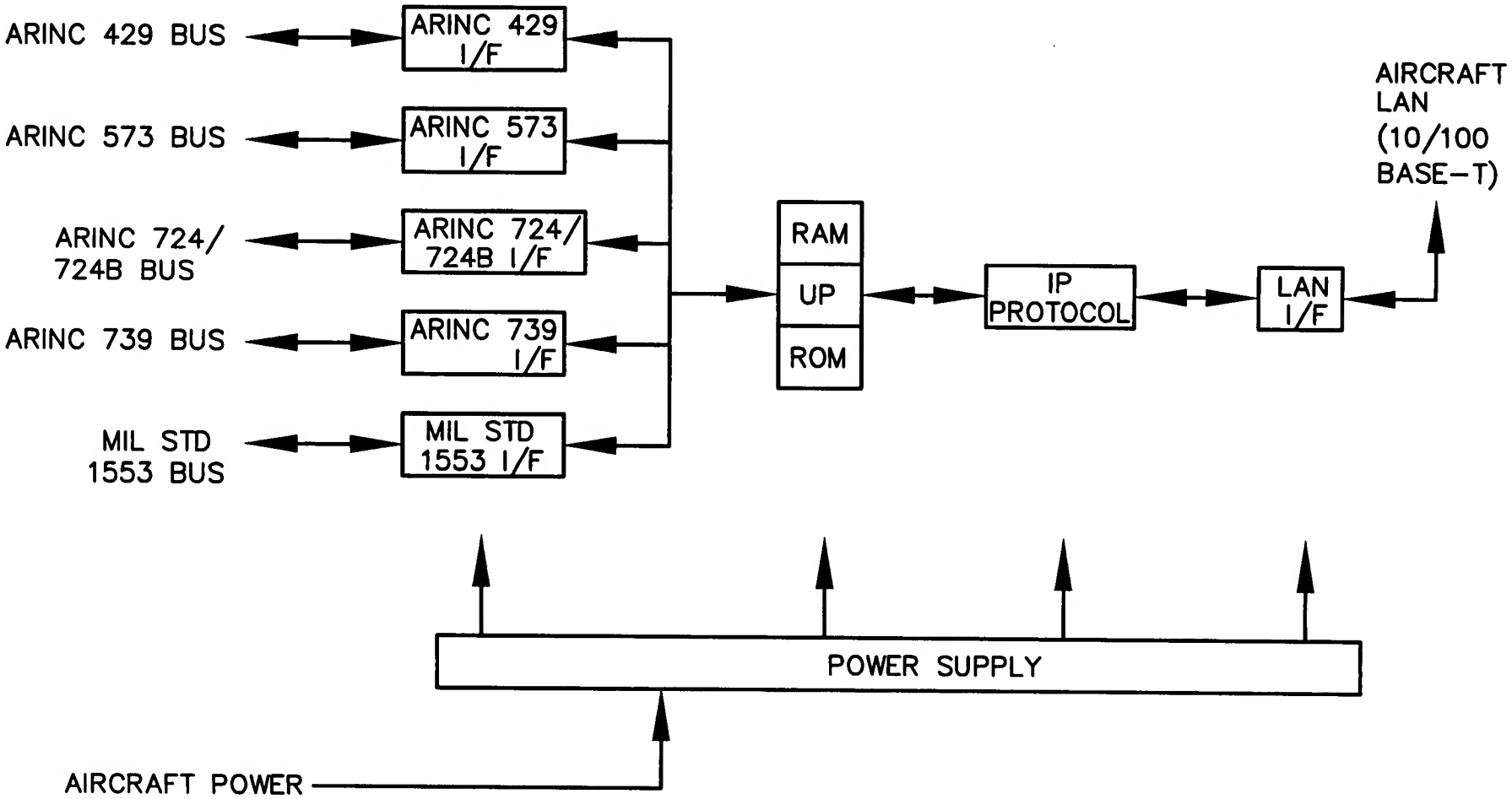
ARINC 429 BUS
ARINC 573 BUS
ARINC 724/
724B BUS
ARINC 739 BUS
MIL STD
1553 BUS
ARINC 429
I/F
ARINC 573
I/F
ARINC 724/
724B I/F
ARINC 739
I/F
MIL STD
1553 I/F
RAM
UP
ROM
IP
PROTOCOL
LAN
I/F
AIRCRAFT
LAN
(10/100
BASE-T)
POWER SUPPLY
AIRCRAFT POWER

FIG. 11

FIG. 16A–16Z

FIG. 17A–17M

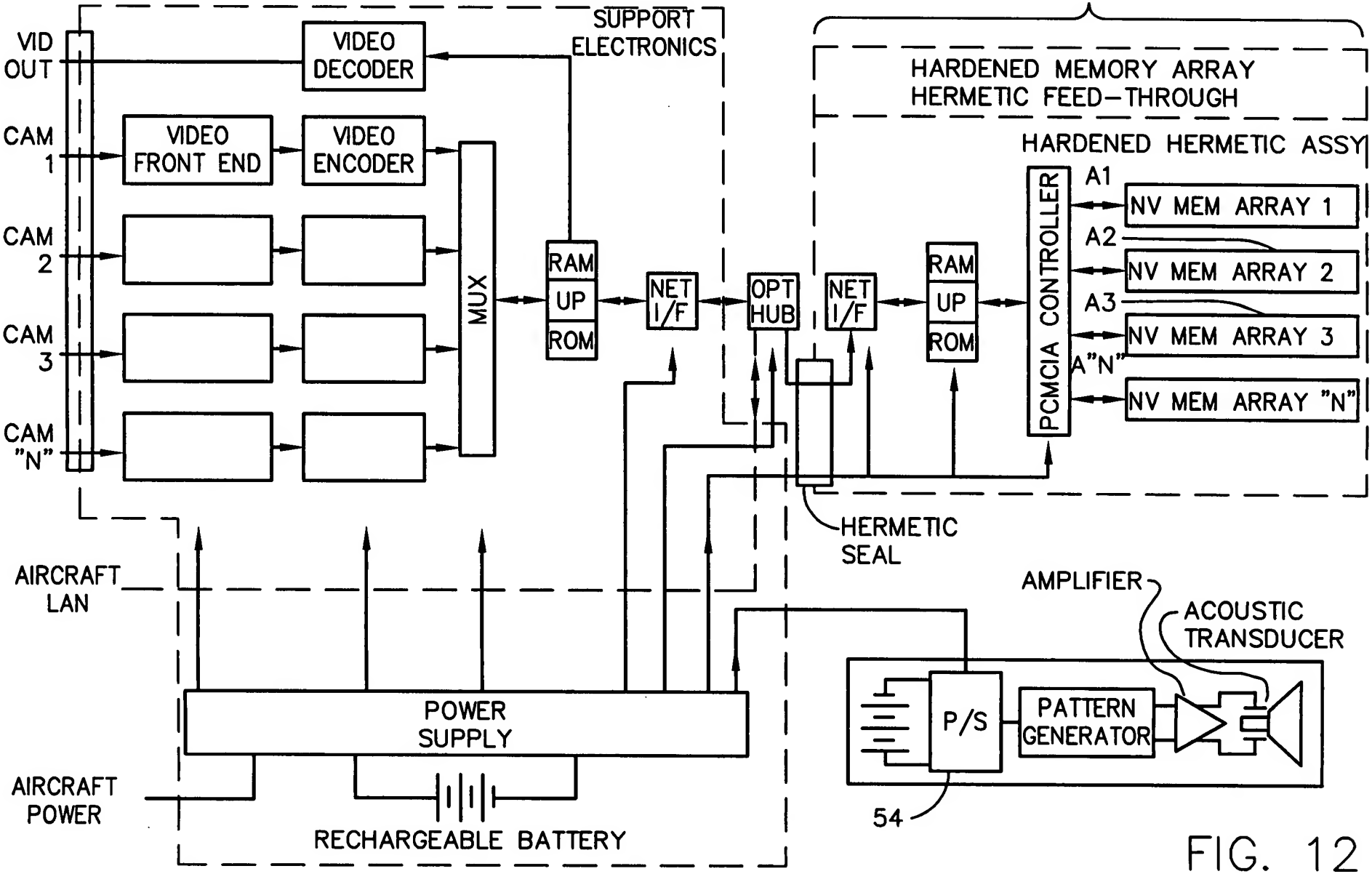

FIG. 12

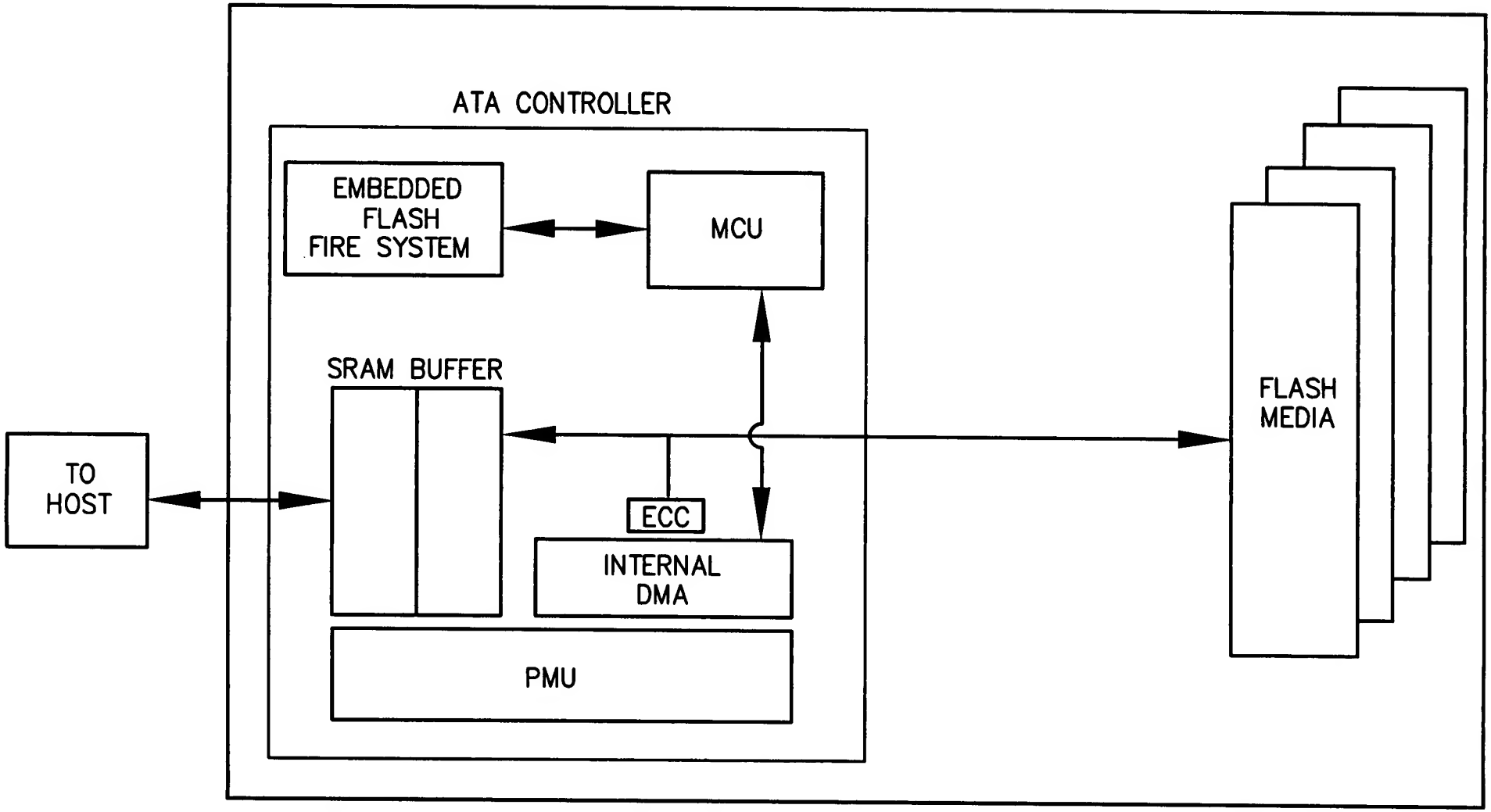
ATA CONTROLLER
EMBEDDED FLASH FIRE SYSTEM
MCU
SRAM BUFFER
TO HOST
ECC
INTERNAL DMA
PMU
FLASH MEDIA

FIG. 13

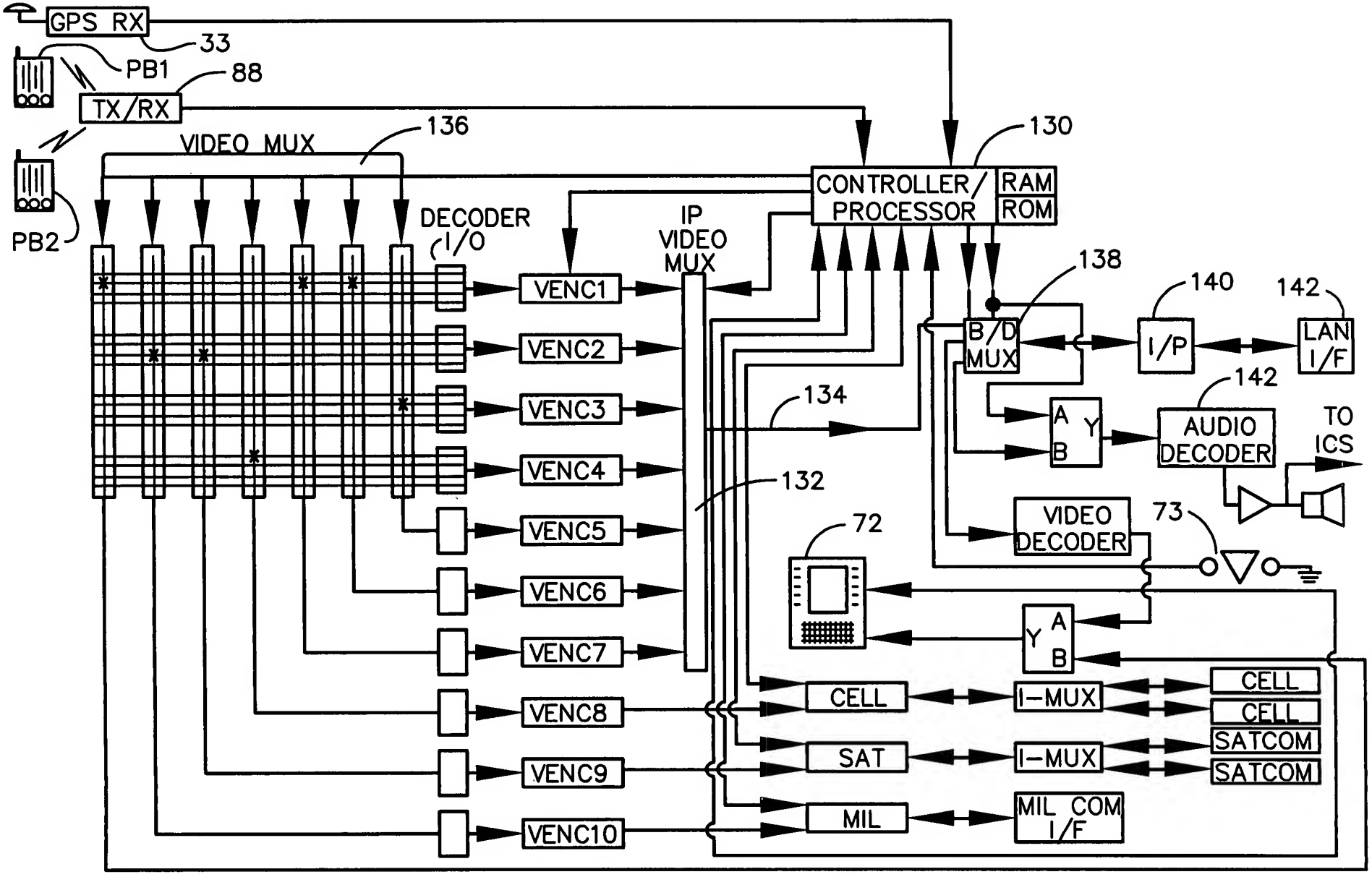
GPS RX
33
PB1
88
TX/RX
PB2
VIDEO MUX
136
DECODER I/O
IP VIDEO MUX
CONTROLLER/ PROCESSOR
RAM
ROM
130
138
140
142
B/D MUX
I/P
LAN I/F
142
AUDIO DECODER
TO ICS
134
132
VENC1
VENC2
VENC3
VENC4
VENC5
VENC6
VENC7
VENC8
VENC9
VENC10
72
VIDEO DECODER
73
CELL
I-MUX
CELL
CELL
SATCOM
SAT
I-MUX
SATCOM
MIL
MIL COM I/F

FIG. 14

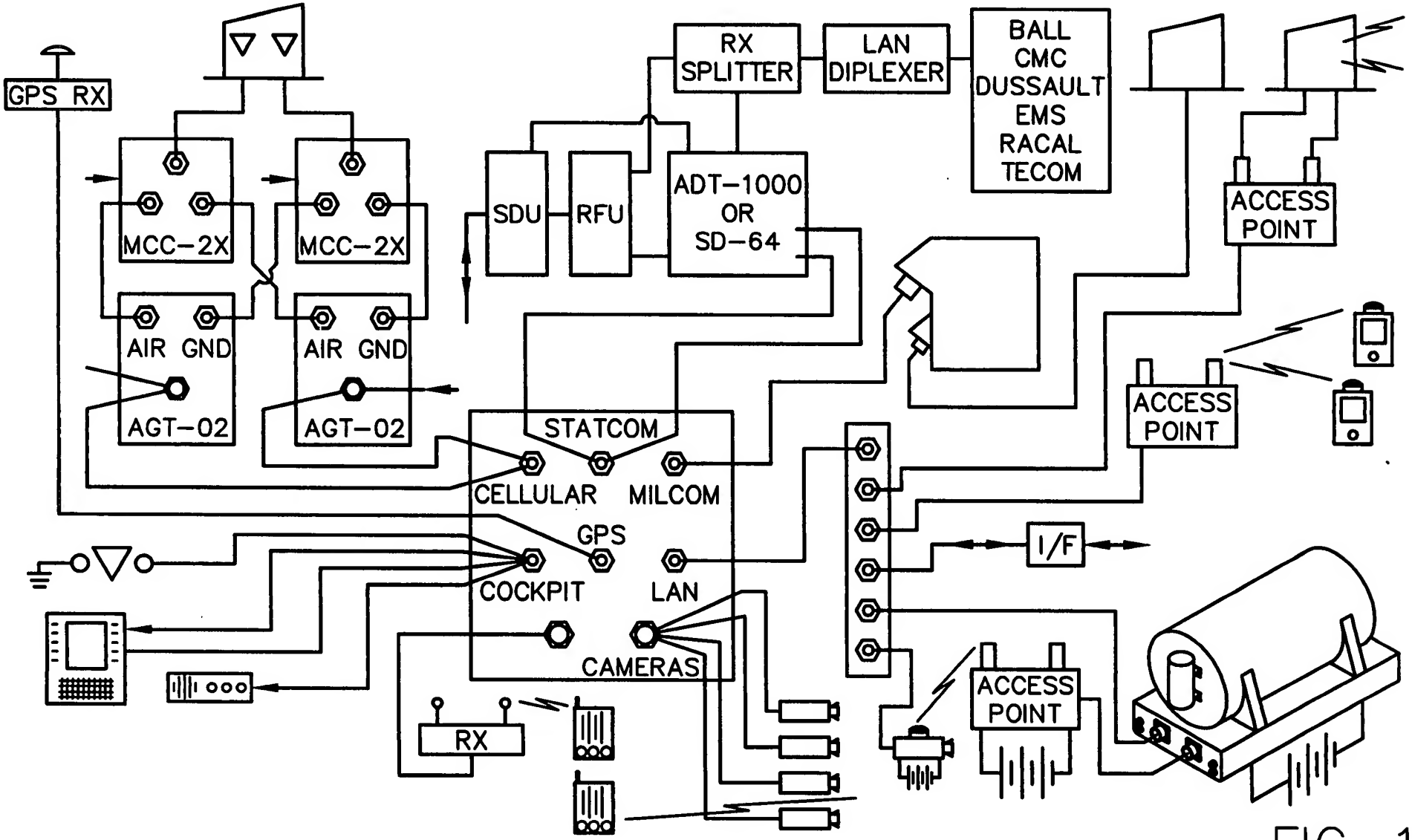
GPS RX
MCC–2X
MCC–2X
AIR GND
AIR GND
AGT–02
AGT–02
SDU
RFU
ADT–1000
OR
SD–64
RX
SPLITTER
LAN
DIPLEXER
BALL
CMC
DUSSAULT
EMS
RACAL
TECOM
ACCESS
POINT
ACCESS
POINT
ACCESS
POINT
STATCOM
CELLULAR
MILCOM
GPS
COCKPIT
LAN
CAMERAS
I/F
RX

FIG. 15

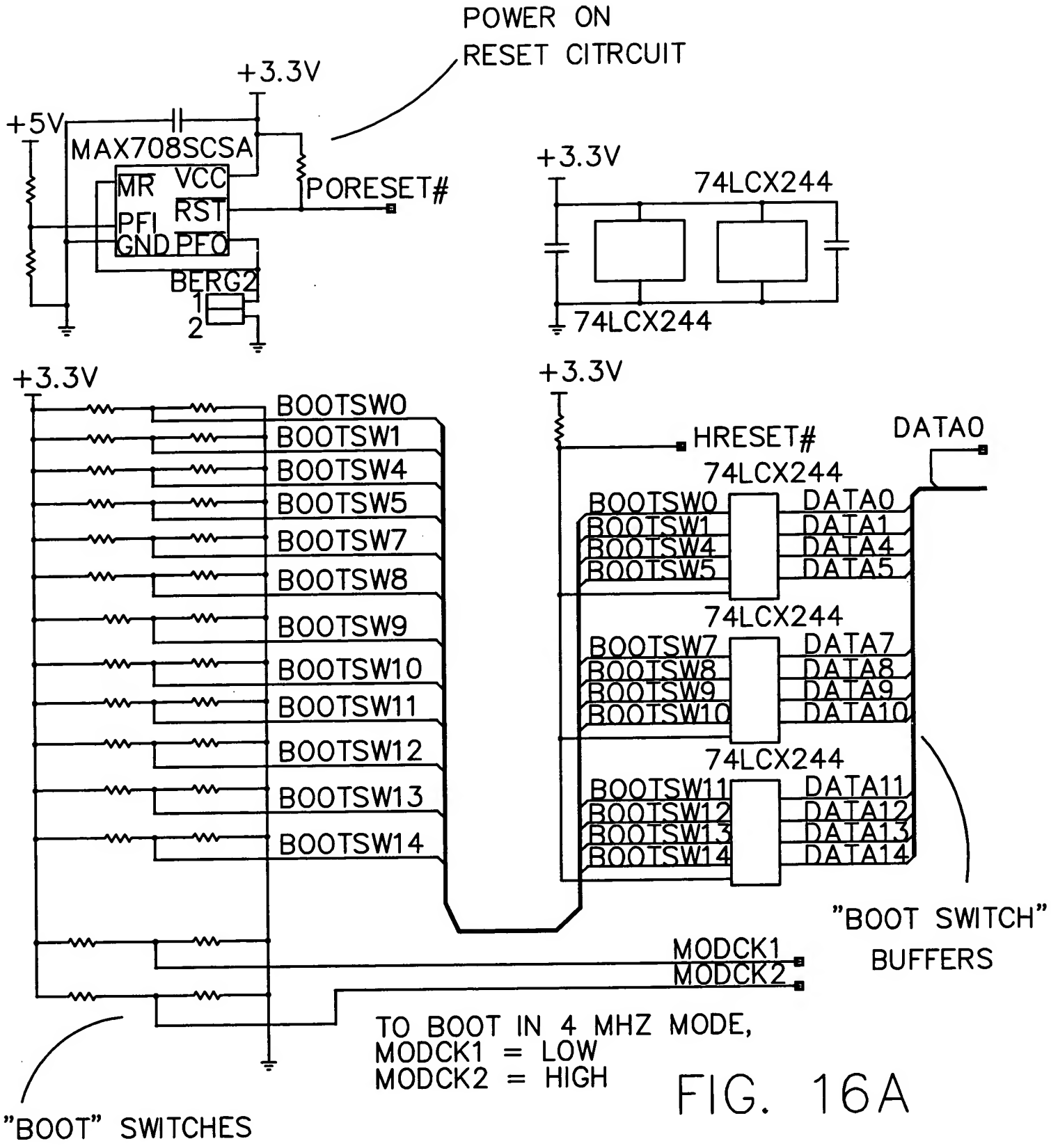
POWER ON
RESET CITRCUIT
+3.3V
+5V
MAX708SCSA
MR
VCC
RST
PFI
GND
PFO
PORESET#
BERG2
1
2
+3.3V
74LCX244
74LCX244
+3.3V
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
+3.3V
HRESET#
DATA0
74LCX244
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
DATA0
DATA1
DATA4
DATA5
74LCX244
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
DATA7
DATA8
DATA9
DATA10
74LCX244
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
DATA11
DATA12
DATA13
DATA14
"BOOT SWITCH"
BUFFERS
MODCK1
MODCK2
TO BOOT IN 4 MHZ MODE,
MODCK1 = LOW
MODCK2 = HIGH
"BOOT" SWITCHES

FIG. 16A

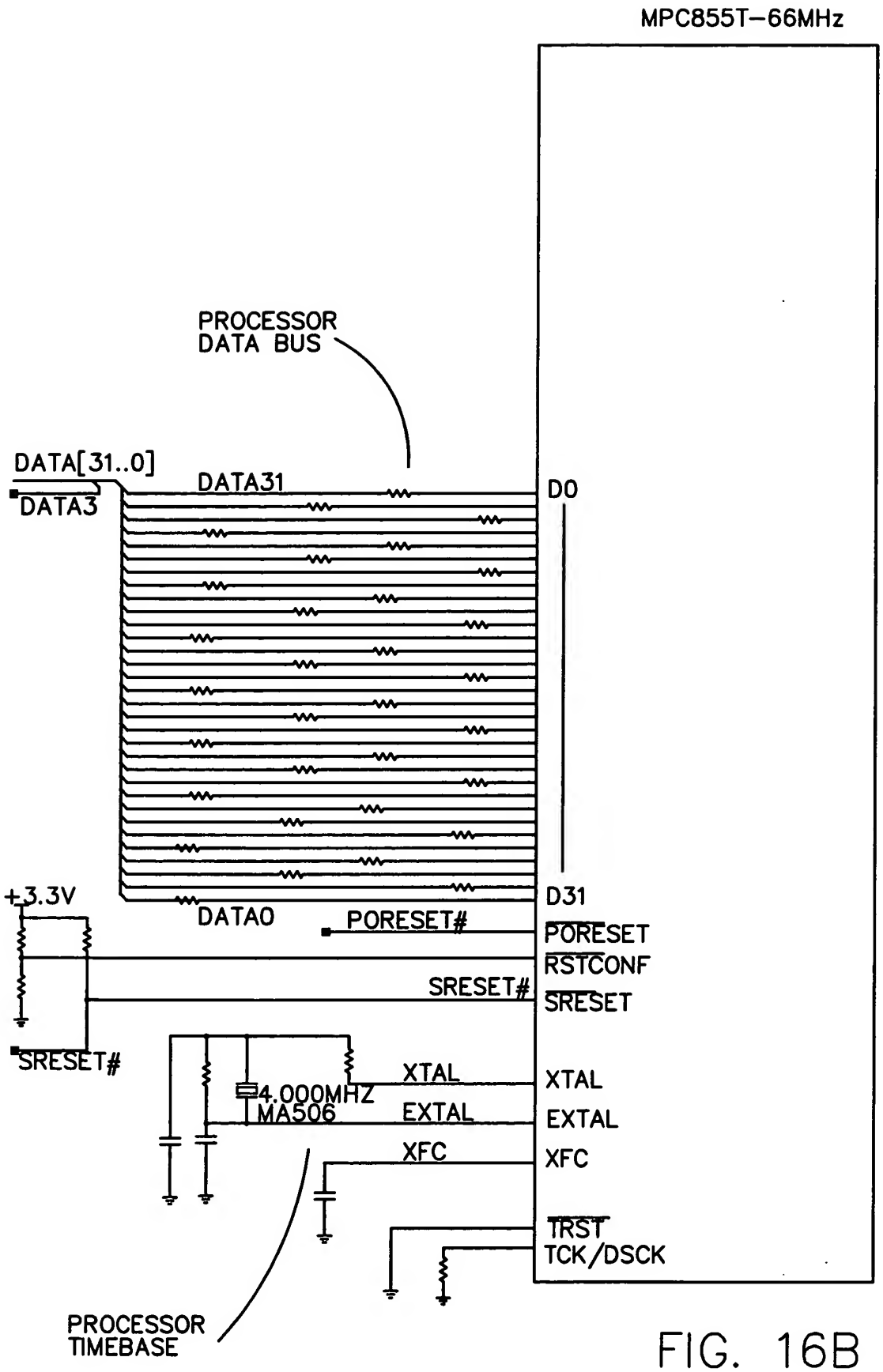
MPC855T–66MHz
PROCESSOR
DATA BUS
DATA[31..0]
DATA31
DATA3
D0
D31
DATA0
+3.3V
PORESET#
PORESET
RSTCONF
SRESET#
SRESET
SRESET#
XTAL
4.000MHZ
MA506
EXTAL
XTAL
EXTAL
XFC
XFC
TRST
TCK/DSCK
PROCESSOR
TIMEBASE

FIG. 16B

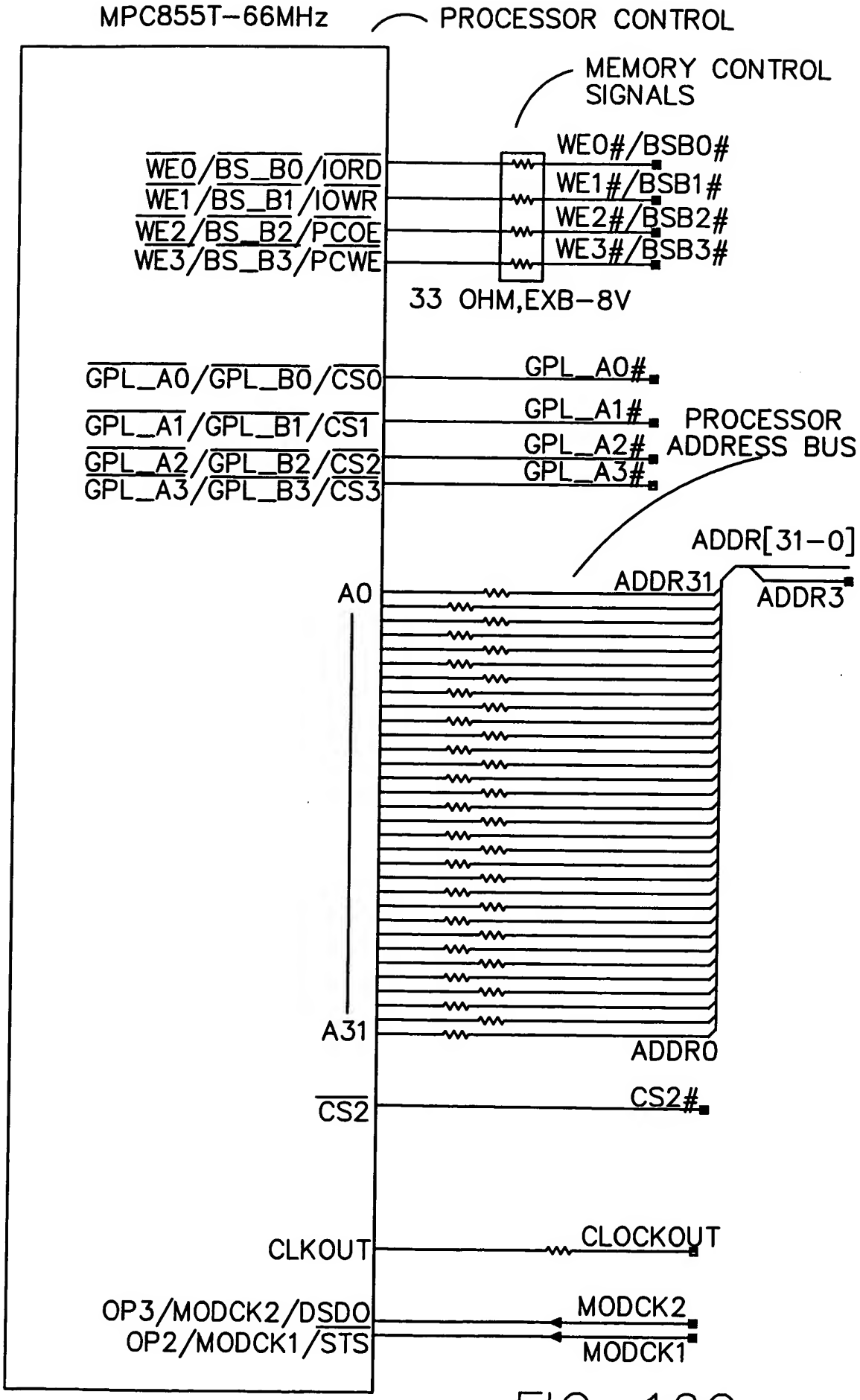
MPC855T-66MHz
PROCESSOR CONTROL
MEMORY CONTROL SIGNALS
WE0/BS_B0/IORD
WE1/BS_B1/IOWR
WE2/BS_B2/PCOE
WE3/BS_B3/PCWE
WE0#/BSB0#
WE1#/BSB1#
WE2#/BSB2#
WE3#/BSB3#
33 OHM,EXB-8V
GPL_A0/GPL_B0/CS0
GPL_A1/GPL_B1/CS1
GPL_A2/GPL_B2/CS2
GPL_A3/GPL_B3/CS3
GPL_A0#
GPL_A1#
GPL_A2#
GPL_A3#
PROCESSOR ADDRESS BUS
ADDR[31-0]
ADDR31
ADDR3
A0
A31
ADDR0
CS2
CS2#
CLKOUT
CLOCKOUT
OP3/MODCK2/DSDO
OP2/MODCK1/STS
MODCK2
MODCK1

FIG. 16C

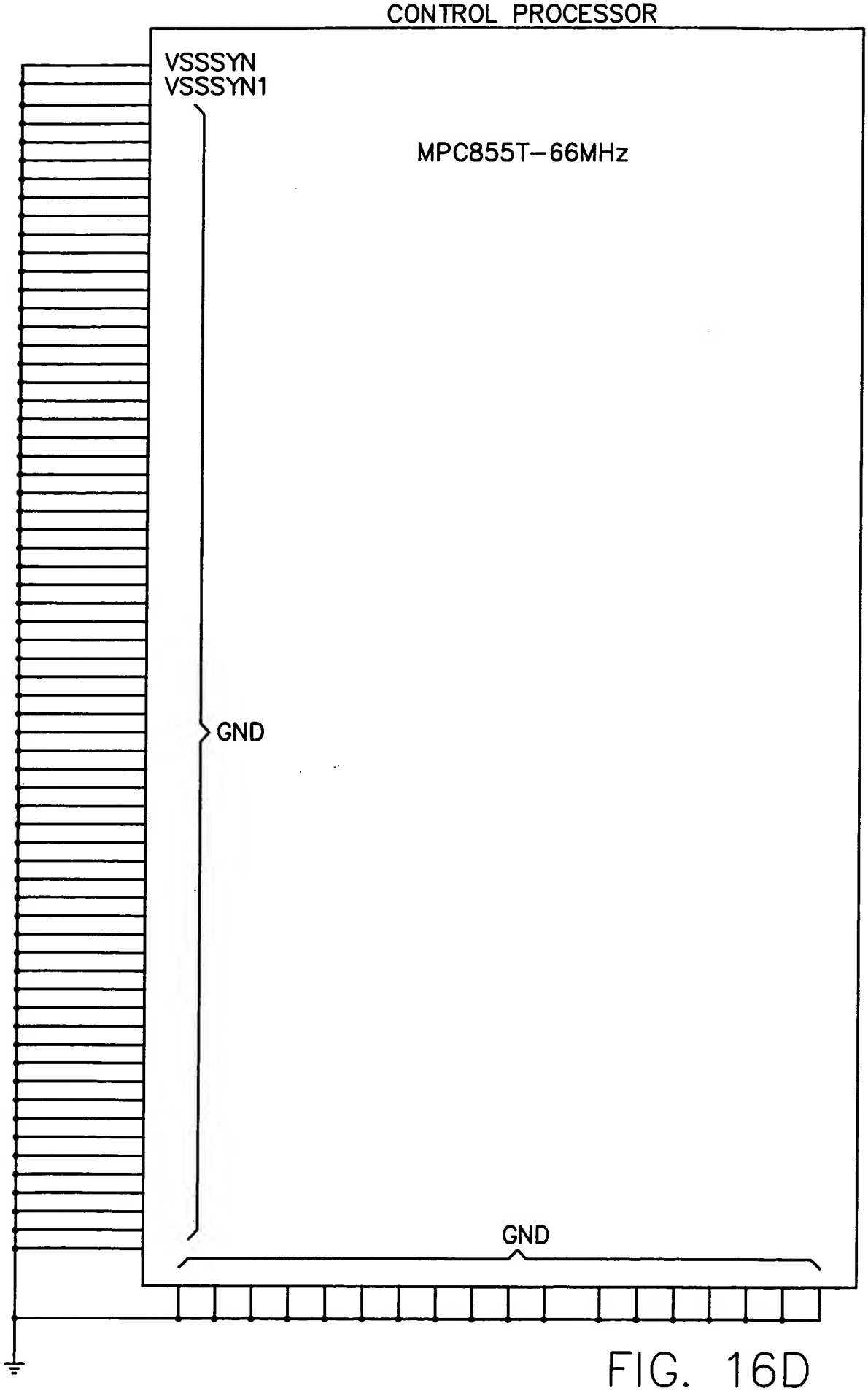

FIG. 16D

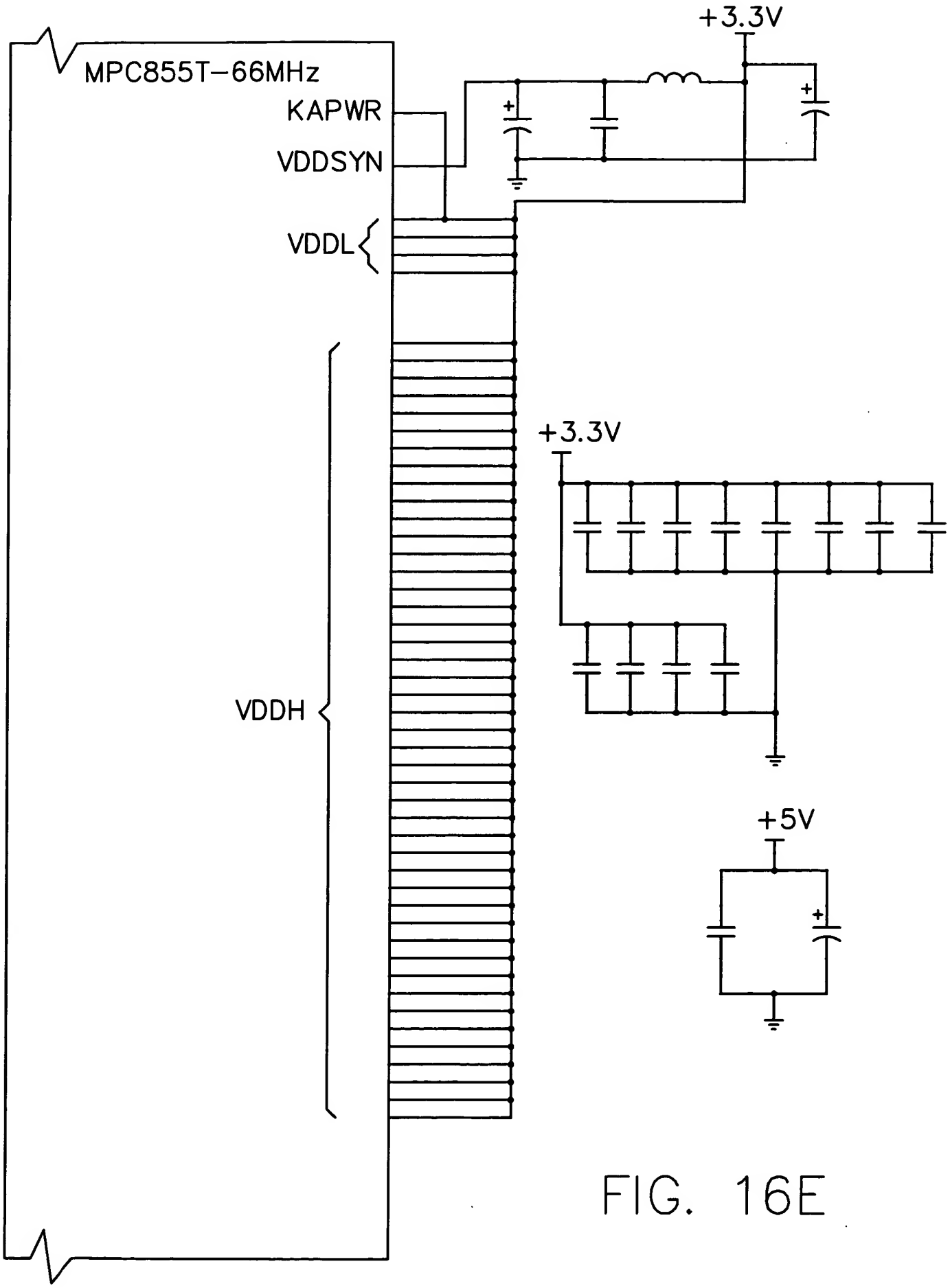

FIG. 16E

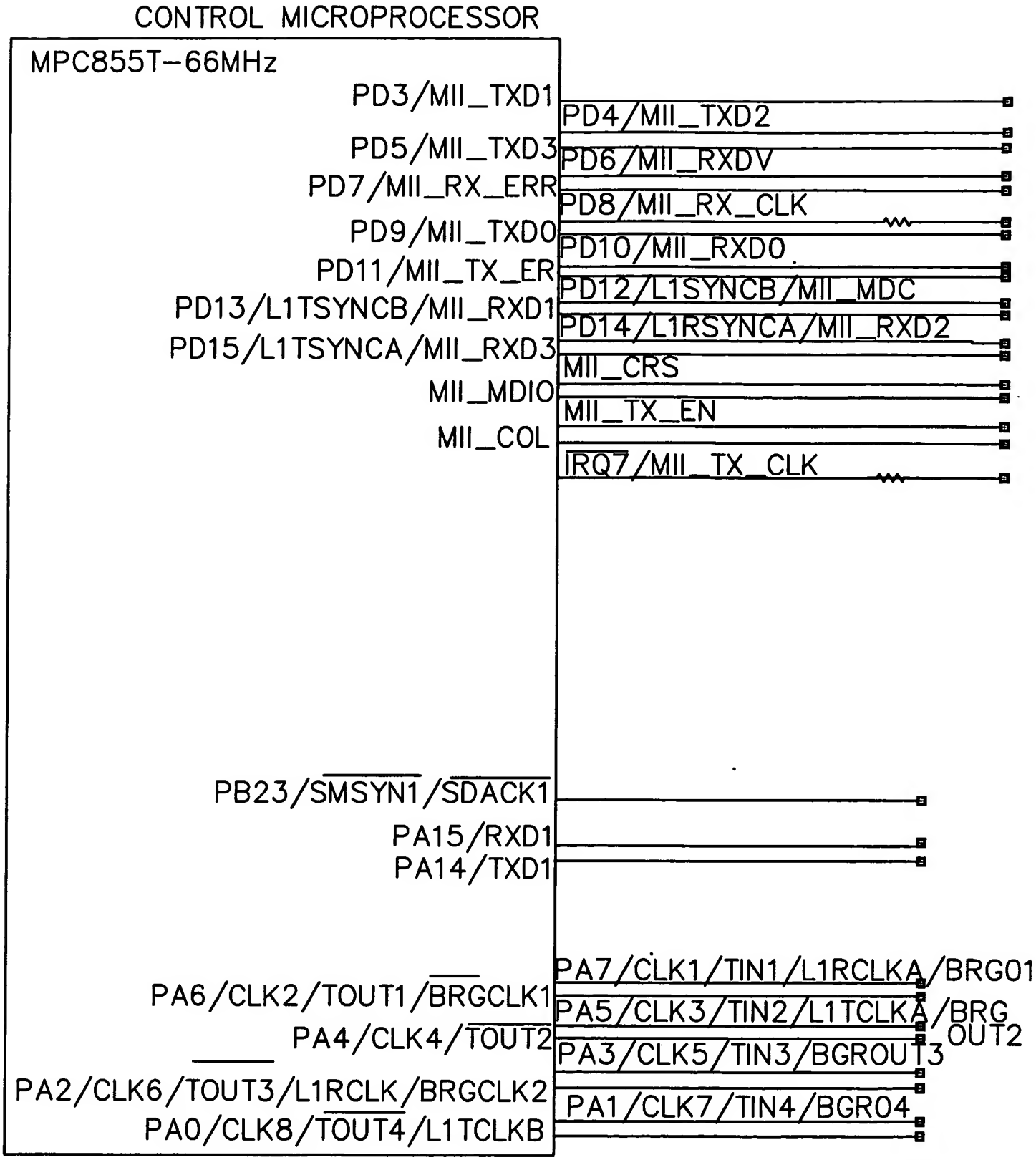
CONTROL MICROPROCESSOR
MPC855T–66MHz
PD3/MII_TXD1
PD4/MII_TXD2
PD5/MII_TXD3
PD6/MII_RXDV
PD7/MII_RX_ERR
PD8/MII_RX_CLK
PD9/MII_TXD0
PD10/MII_RXD0
PD11/MII_TX_ER
PD12/L1SYNCB/MII_MDC
PD13/L1TSYNCB/MII_RXD1
PD14/L1RSYNCA/MII_RXD2
PD15/L1TSYNCA/MII_RXD3
MII_CRS
MII_MDIO
MII_TX_EN
MII_COL
IRQ7/MII_TX_CLK
PB23/SMSYN1/SDACK1
PA15/RXD1
PA14/TXD1
PA7/CLK1/TIN1/L1RCLKA/BRG01
PA6/CLK2/TOUT1/BRGCLK1
PA5/CLK3/TIN2/L1TCLKA/BRG
PA4/CLK4/TOUT2
OUT2
PA3/CLK5/TIN3/BGROUT3
PA2/CLK6/TOUT3/L1RCLK/BRGCLK2
PA1/CLK7/TIN4/BGR04
PA0/CLK8/TOUT4/L1TCLKB

FIG. 16F

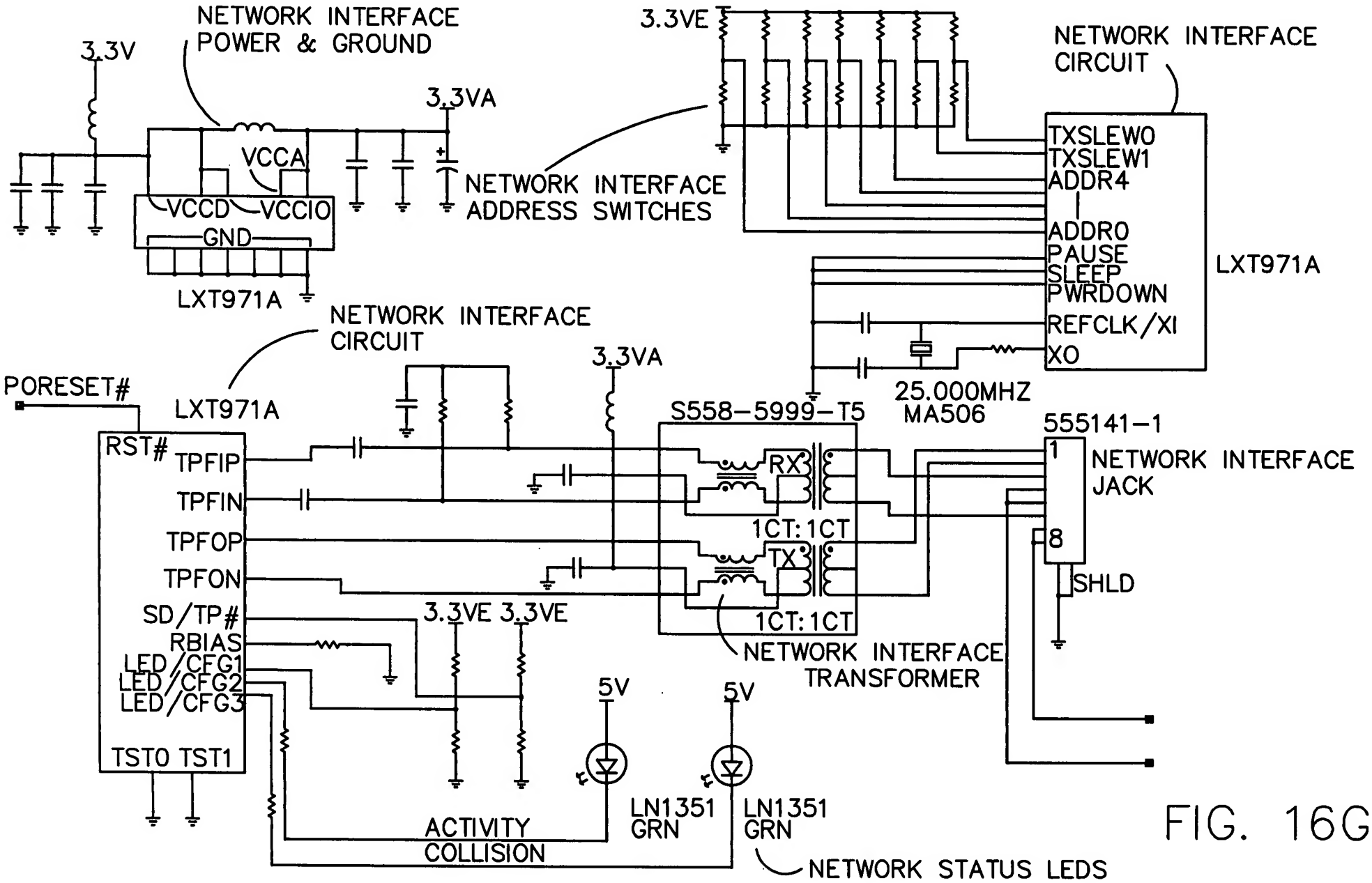
NETWORK INTERFACE
POWER & GROUND
3.3V
3.3VA
VCCA
VCCD
VCCIO
GND
LXT971A
3.3VE
NETWORK INTERFACE
ADDRESS SWITCHES
NETWORK INTERFACE
CIRCUIT
TXSLEW0
TXSLEW1
ADDR4
ADDR0
PAUSE
SLEEP
PWRDOWN
REFCLK/XI
XO
LXT971A
25.000MHZ
MA506
NETWORK INTERFACE
CIRCUIT
LXT971A
PORESET#
RST#
TPFIP
TPFIN
TPFOP
TPFON
SD/TP#
RBIAS
LED/CFG1
LED/CFG2
LED/CFG3
TST0 TST1
3.3VA
3.3VE 3.3VE
S558-5999-T5
RX
1CT:1CT
TX
1CT:1CT
NETWORK INTERFACE
TRANSFORMER
555141-1
1
8
SHLD
NETWORK INTERFACE
JACK
5V
5V
LN1351
GRN
LN1351
GRN
ACTIVITY
COLLISION
NETWORK STATUS LEDS

FIG. 16G

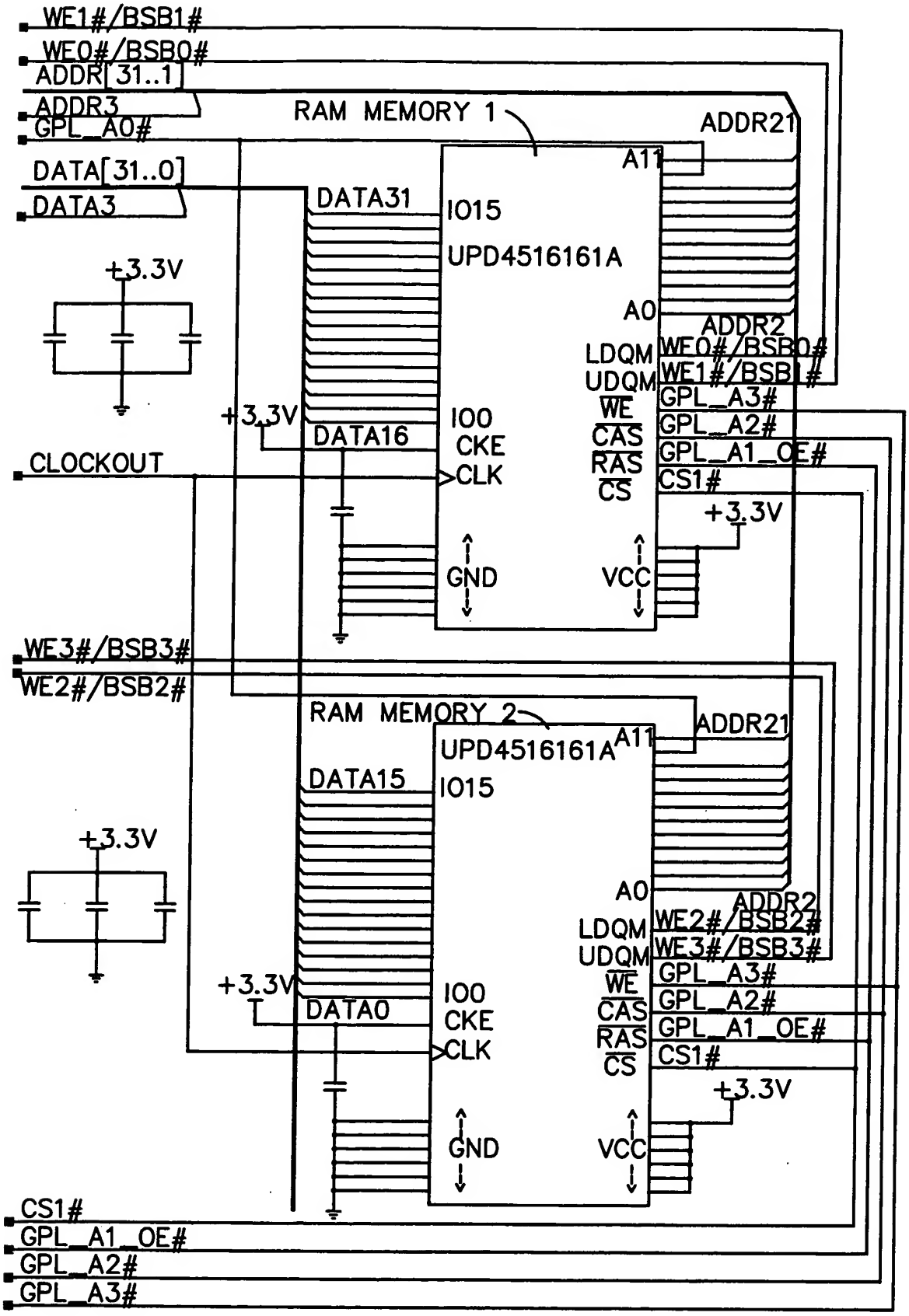
WE1#/BSB1#
WE0#/BSB0#
ADDR[31..1]
ADDR3
GPL_A0#
DATA[31..0]
DATA3
RAM MEMORY 1
ADDR21
A11
DATA31
IO15
UPD4516161A
A0
ADDR2
LDQM
WE0#/BSB0#
UDQM
WE1#/BSB1#
WE
GPL_A3#
CAS
GPL_A2#
RAS
GPL_A1_OE#
CS
CS1#
+3.3V
IO0
DATA16
CKE
CLK
CLOCKOUT
GND
VCC
WE3#/BSB3#
WE2#/BSB2#
RAM MEMORY 2
ADDR21
UPD4516161A
A11
DATA15
IO15
A0
ADDR2
LDQM
WE2#/BSB2#
UDQM
WE3#/BSB3#
WE
GPL_A3#
CAS
GPL_A2#
RAS
GPL_A1_OE#
CS
CS1#
+3.3V
IO0
DATA0
CKE
CLK
GND
VCC
CS1#
GPL_A1_OE#
GPL_A2#
GPL_A3#

FIG. 16H

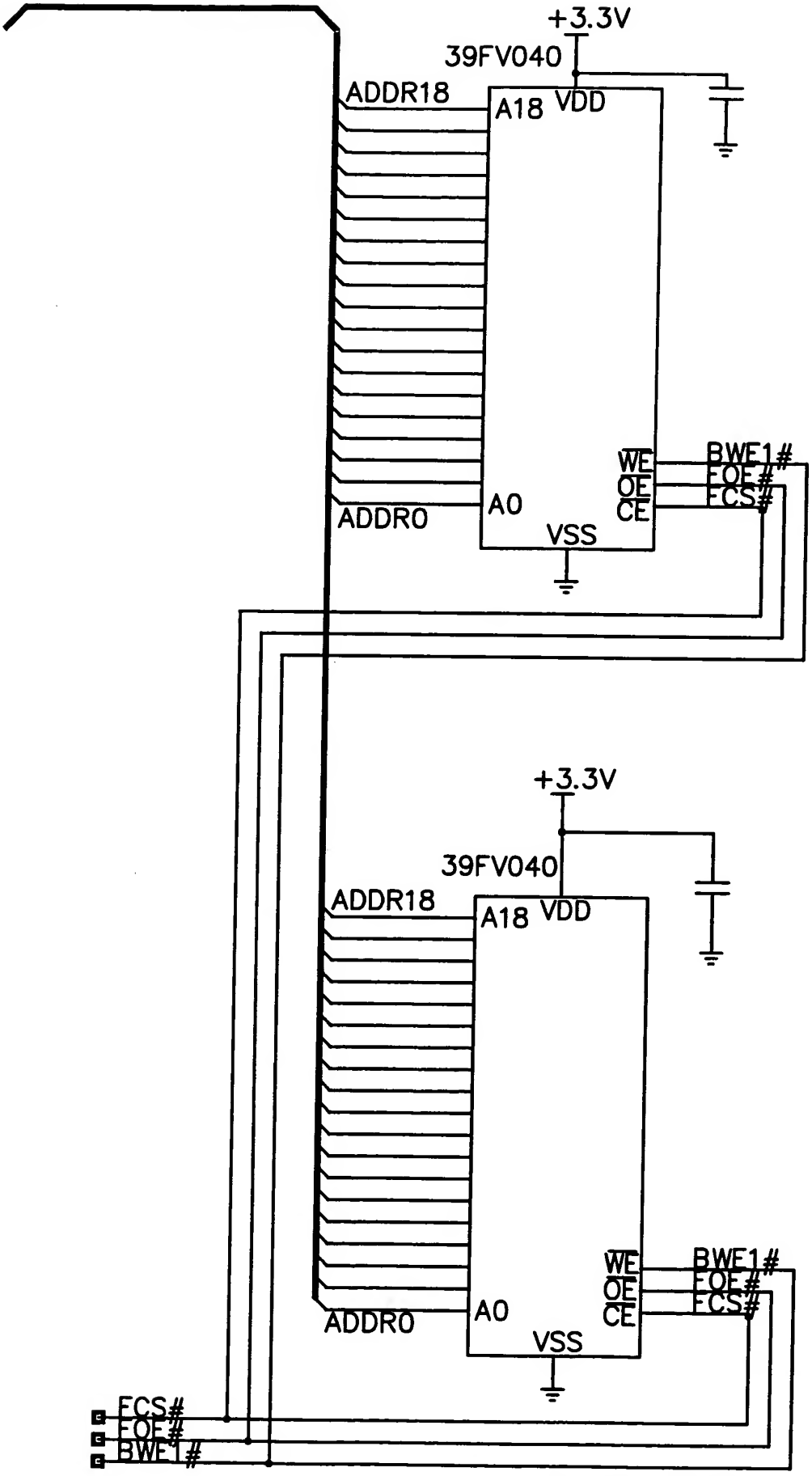
+3.3V
39FV040
ADDR18
A18
VDD
WE
OE
CE
BWE1#
FOE#
FCS#
ADDR0
A0
VSS
+3.3V
39FV040
ADDR18
A18
VDD
WE
OE
CE
BWE1#
FOE#
FCS#
ADDR0
A0
VSS
FCS#
FOE#
BWE1#

FIG. 16I

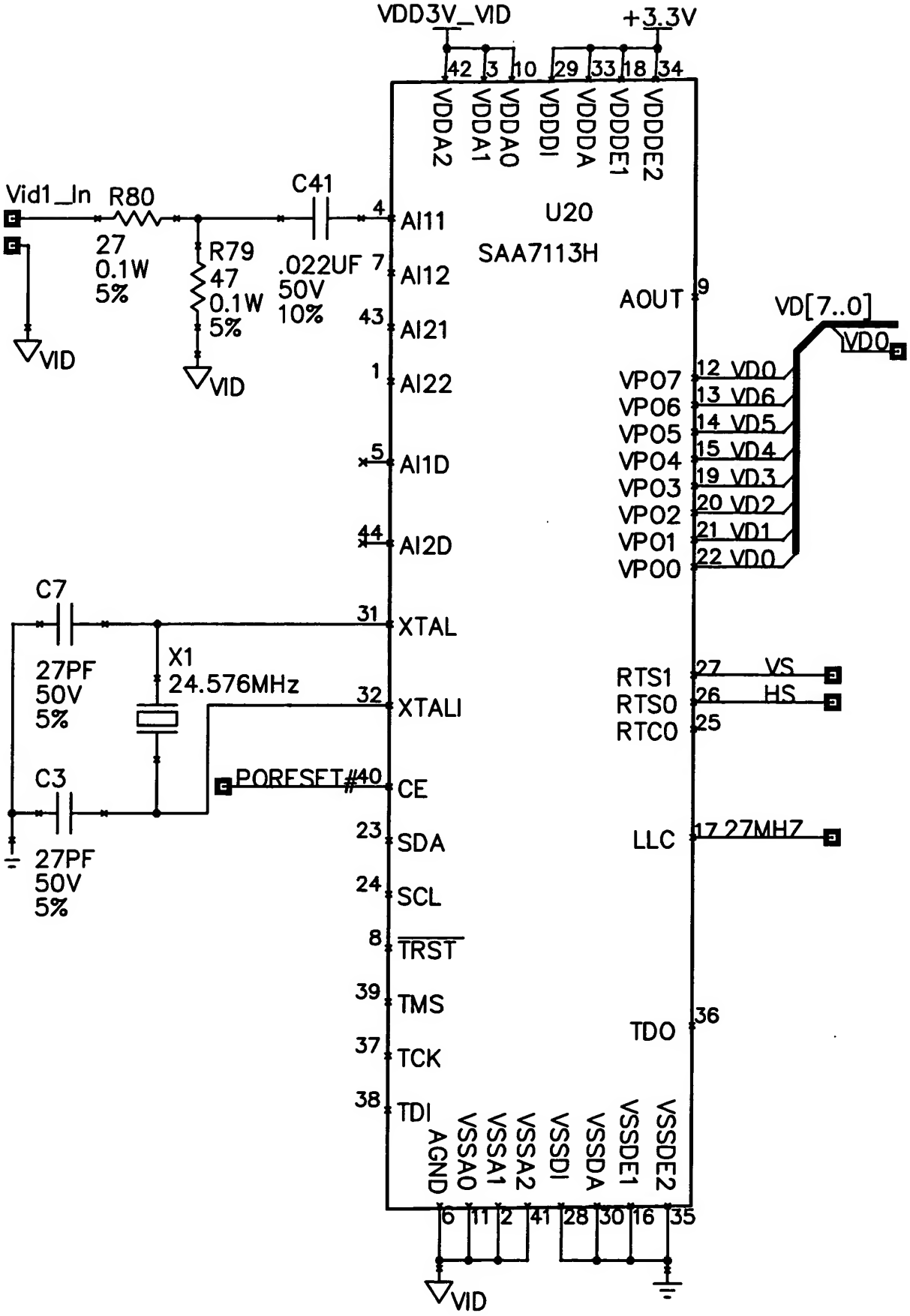
VDD3V_VID
+3.3V
42 3 10 29 33 18 34
VDDA2 VDDA1 VDDA0 VDDDI VDDDA VDDDE1 VDDDE2
U20
SAA7113H
Vid1_In
R80
27
0.1W
5%
R79
47
0.1W
5%
C41
.022UF
50V
10%
VID
4 AI11
7 AI12
43 AI21
1 AI22
5 AI1D
44 AI2D
31 XTAL
32 XTALI
40 CE
23 SDA
24 SCL
8 TRST
39 TMS
37 TCK
38 TDI
AOUT 9
VD[7..0]
VD0
VP07 12 VD0
VP06 13 VD6
VP05 14 VD5
VP04 15 VD4
VP03 19 VD3
VP02 20 VD2
VP01 21 VD1
VP00 22 VD0
C7
27PF
50V
5%
X1
24.576MHz
C3
27PF
50V
5%
PORESET#
RTS1 27 VS
RTS0 26 HS
RTC0 25
LLC 17 27MHZ
TDO 36
AGND VSSA0 VSSA1 VSSA2 VSSDI VSSDA VSSDE1 VSSDE2
6 11 2 41 28 30 16 35
VID

FIG. 16J

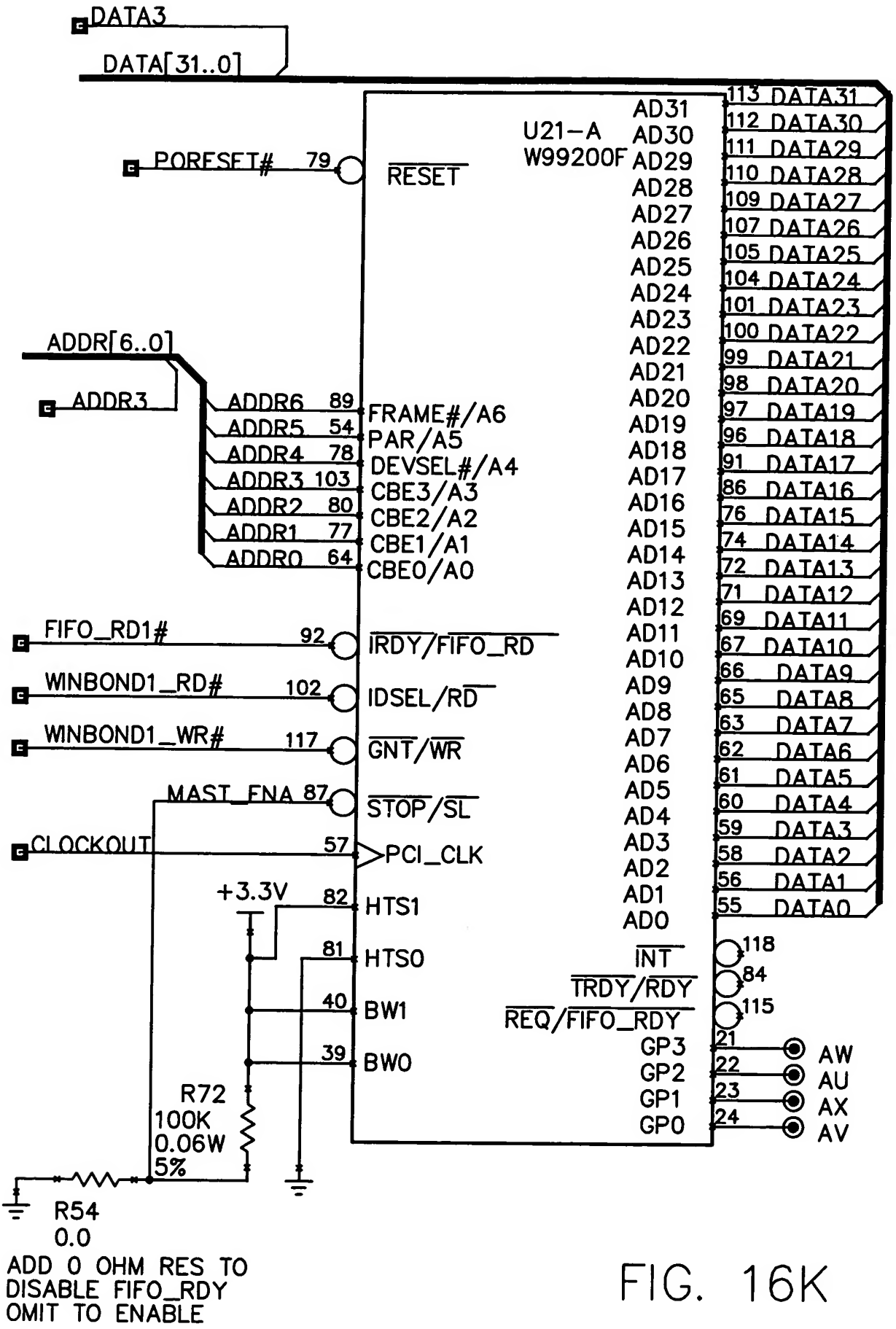
DATA3
DATA[31..0]
PORESET#
79
RESET
U21-A
W99200F
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
113 DATA31
112 DATA30
111 DATA29
110 DATA28
109 DATA27
107 DATA26
105 DATA25
104 DATA24
101 DATA23
100 DATA22
99 DATA21
98 DATA20
97 DATA19
96 DATA18
91 DATA17
86 DATA16
76 DATA15
74 DATA14
72 DATA13
71 DATA12
69 DATA11
67 DATA10
66 DATA9
65 DATA8
63 DATA7
62 DATA6
61 DATA5
60 DATA4
59 DATA3
58 DATA2
56 DATA1
55 DATA0
ADDR[6..0]
ADDR3
ADDR6 89
ADDR5 54
ADDR4 78
ADDR3 103
ADDR2 80
ADDR1 77
ADDR0 64
FRAME#/A6
PAR/A5
DEVSEL#/A4
CBE3/A3
CBE2/A2
CBE1/A1
CBE0/A0
FIFO_RD1#
92
IRDY/FIFO_RD
WINBOND1_RD#
102
IDSEL/RD
WINBOND1_WR#
117
GNT/WR
MAST_ENA 87
STOP/SL
CLOCKOUT
57
PCI_CLK
+3.3V
82
HTS1
81
HTS0
40
BW1
39
BW0
INT
118
TRDY/RDY
84
REQ/FIFO_RDY
115
GP3
GP2
GP1
GP0
21
22
23
24
AW
AU
AX
AV
R72
100K
0.06W
5%
R54
0.0
ADD 0 OHM RES TO
DISABLE FIFO_RDY
OMIT TO ENABLE

FIG. 16K

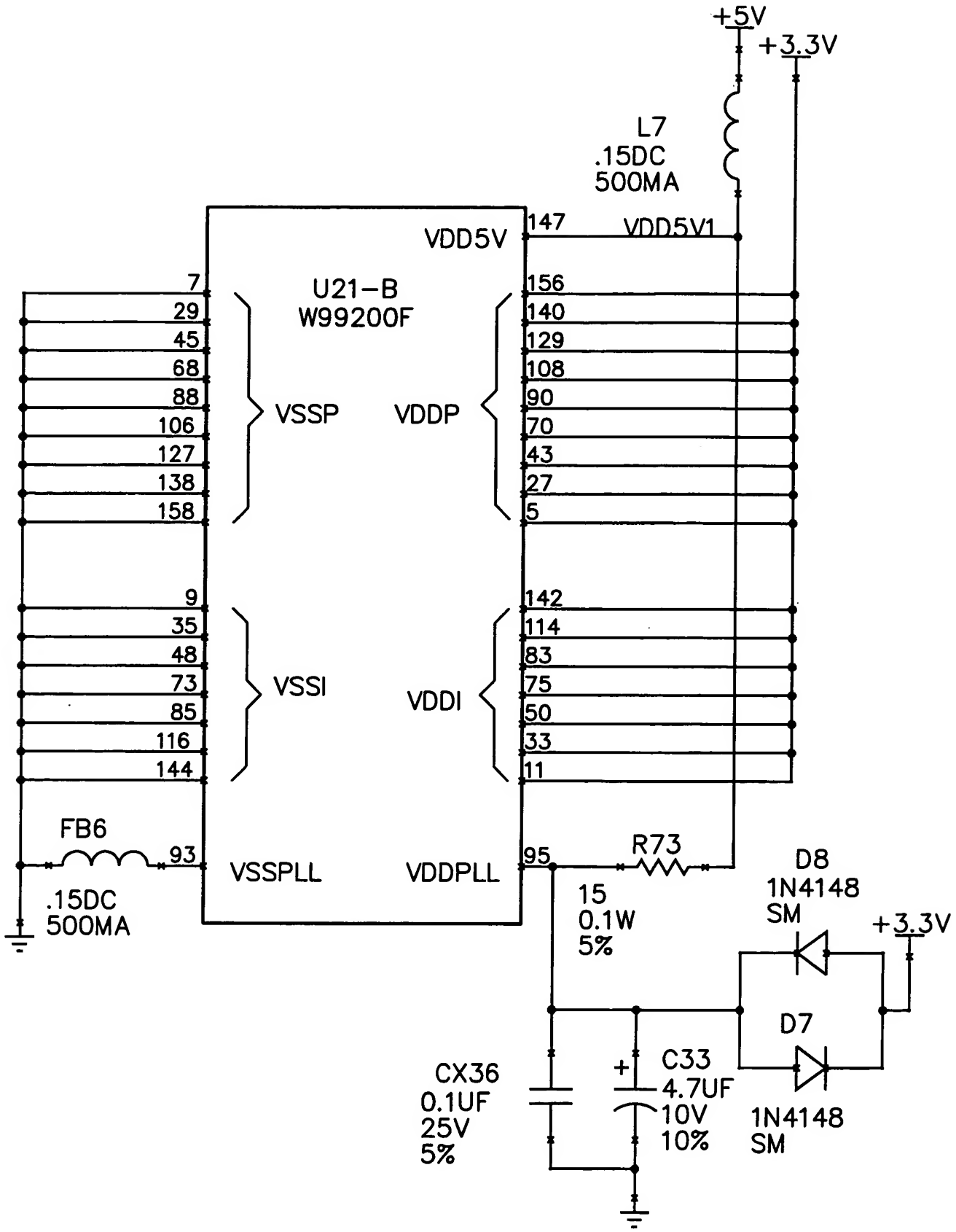
+5V
+3.3V
L7
.15DC
500MA
U21-B
W99200F
VDD5V
147
VDD5V1
7
29
45
68
88
106
127
138
158
VSSP
VDDP
156
140
129
108
90
70
43
27
5
9
35
48
73
85
116
144
VSSI
VDDI
142
114
83
75
50
33
11
FB6
93
VSSPLL
VDDPLL
95
R73
15
0.1W
5%
D8
1N4148
SM
+3.3V
D7
1N4148
SM
CX36
0.1UF
25V
5%
C33
4.7UF
10V
10%
.15DC
500MA

FIG. 16L

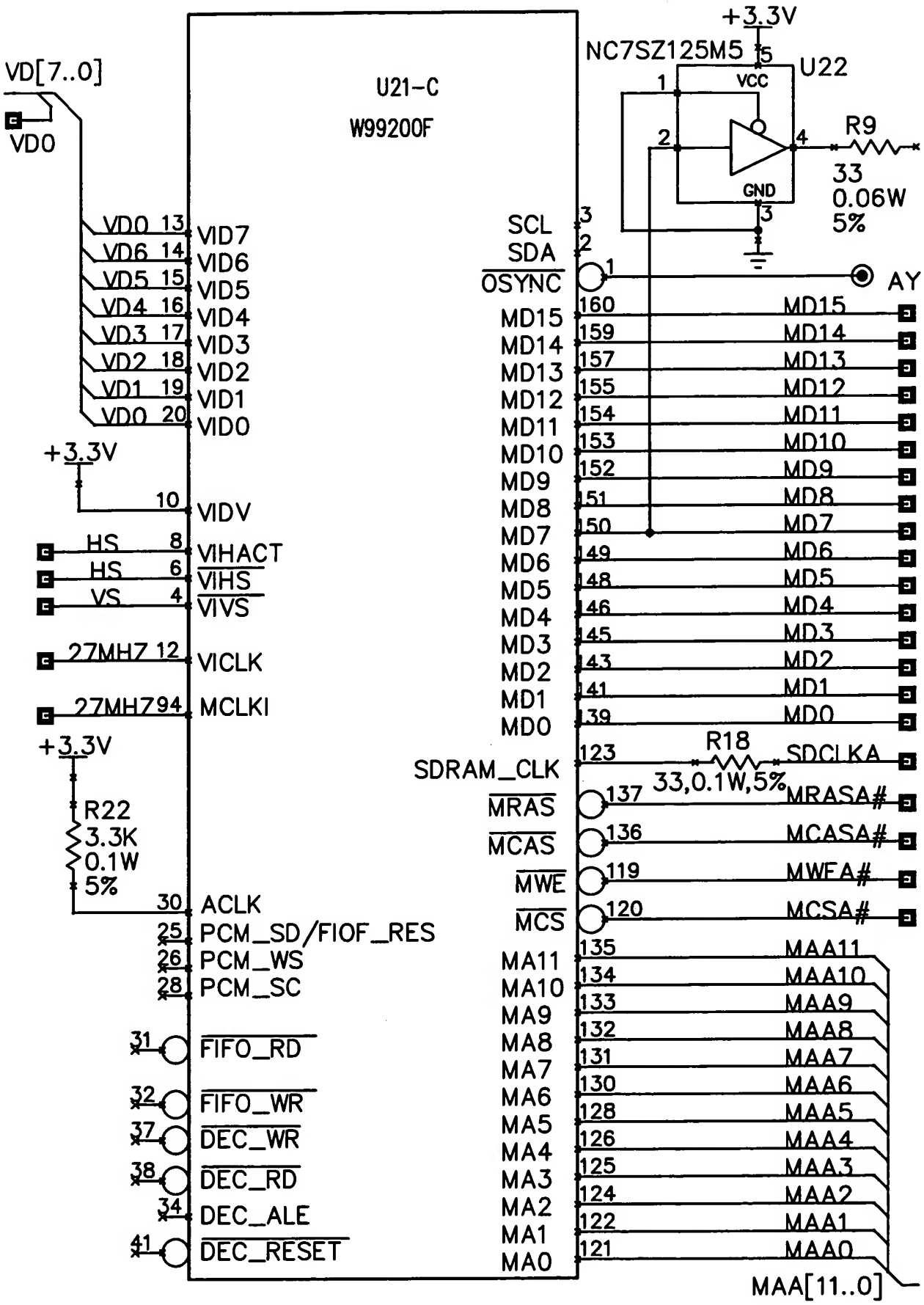
U21-C
W99200F
VD[7..0]
VD0
VD0 13 VID7
VD6 14 VID6
VD5 15 VID5
VD4 16 VID4
VD3 17 VID3
VD2 18 VID2
VD1 19 VID1
VD0 20 VID0
+3.3V
10 VIDV
HS 8 VIHACT
HS 6 VIHS
VS 4 VIVS
27MHZ 12 VICLK
27MHZ 94 MCLKI
+3.3V
R22
3.3K
0.1W
5%
30 ACLK
25 PCM_SD/FIOF_RES
26 PCM_WS
28 PCM_SC
31 FIFO_RD
32 FIFO_WR
37 DEC_WR
38 DEC_RD
34 DEC_ALE
41 DEC_RESET
SCL 3
SDA 2
OSYNC 1
AY
MD15 160
MD14 159
MD13 157
MD12 155
MD11 154
MD10 153
MD9 152
MD8 151
MD7 150
MD6 149
MD5 148
MD4 146
MD3 145
MD2 143
MD1 141
MD0 139
SDRAM_CLK 123
R18
33,0.1W,5%
SDCLKA
MRAS 137
MRASA#
MCAS 136
MCASA#
MWE 119
MWEA#
MCS 120
MCSA#
MA11 135
MA10 134
MA9 133
MA8 132
MA7 131
MA6 130
MA5 128
MA4 126
MA3 125
MA2 124
MA1 122
MA0 121
MAA11
MAA10
MAA9
MAA8
MAA7
MAA6
MAA5
MAA4
MAA3
MAA2
MAA1
MAA0
MAA[11..0]
+3.3V
NC7SZ125M5
U22
VCC
GND
R9
33
0.06W
5%

FIG. 16M

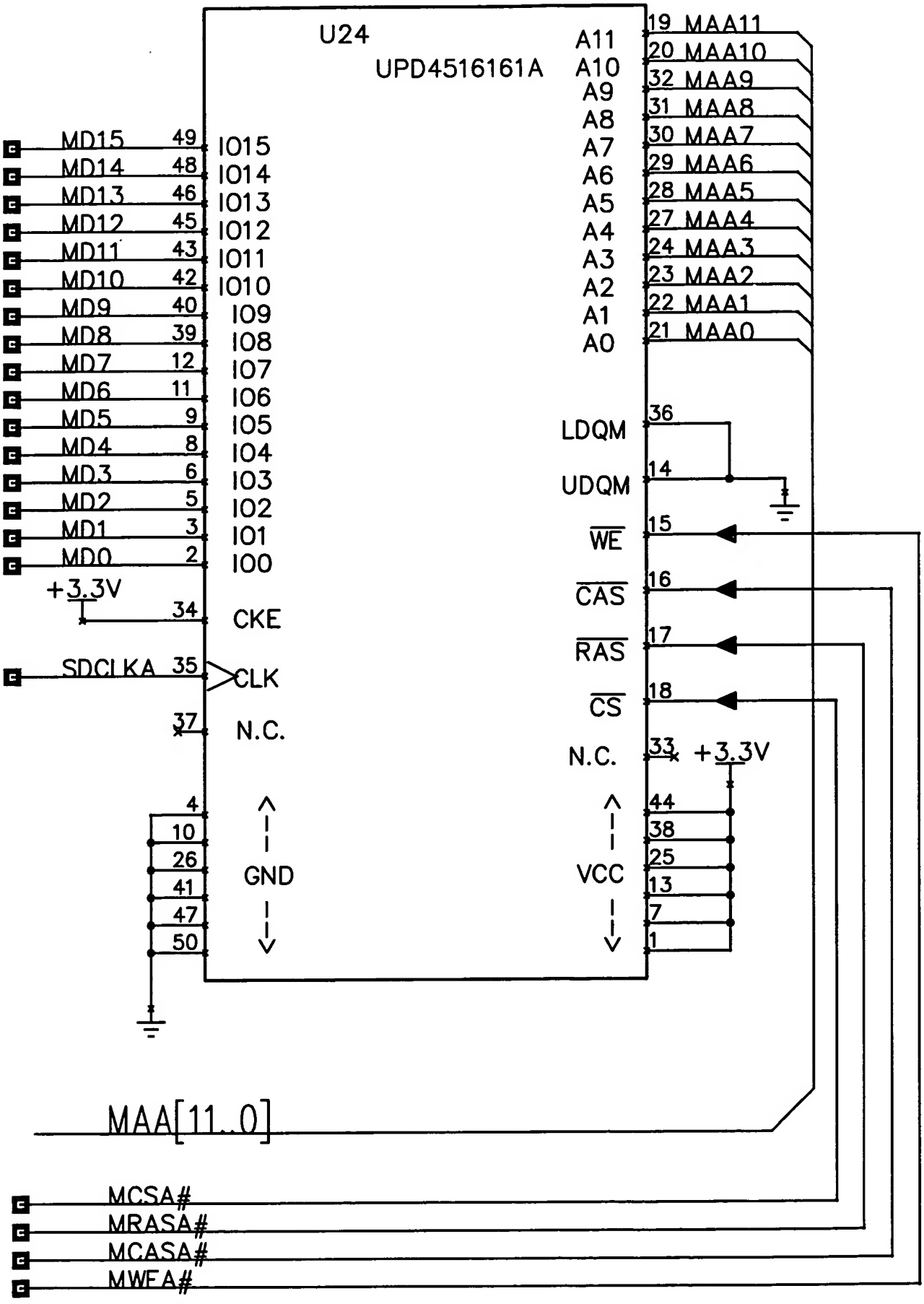
U24
UPD4516161A
MD15
MD14
MD13
MD12
MD11
MD10
MD9
MD8
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
+3.3V
SDCLKA
CKE
CLK
N.C.
GND
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
LDQM
UDQM
WE
CAS
RAS
CS
N.C.
+3.3V
VCC
MAA[11..0]
MCSA#
MRASA#
MCASA#
MWEA#

FIG. 16N

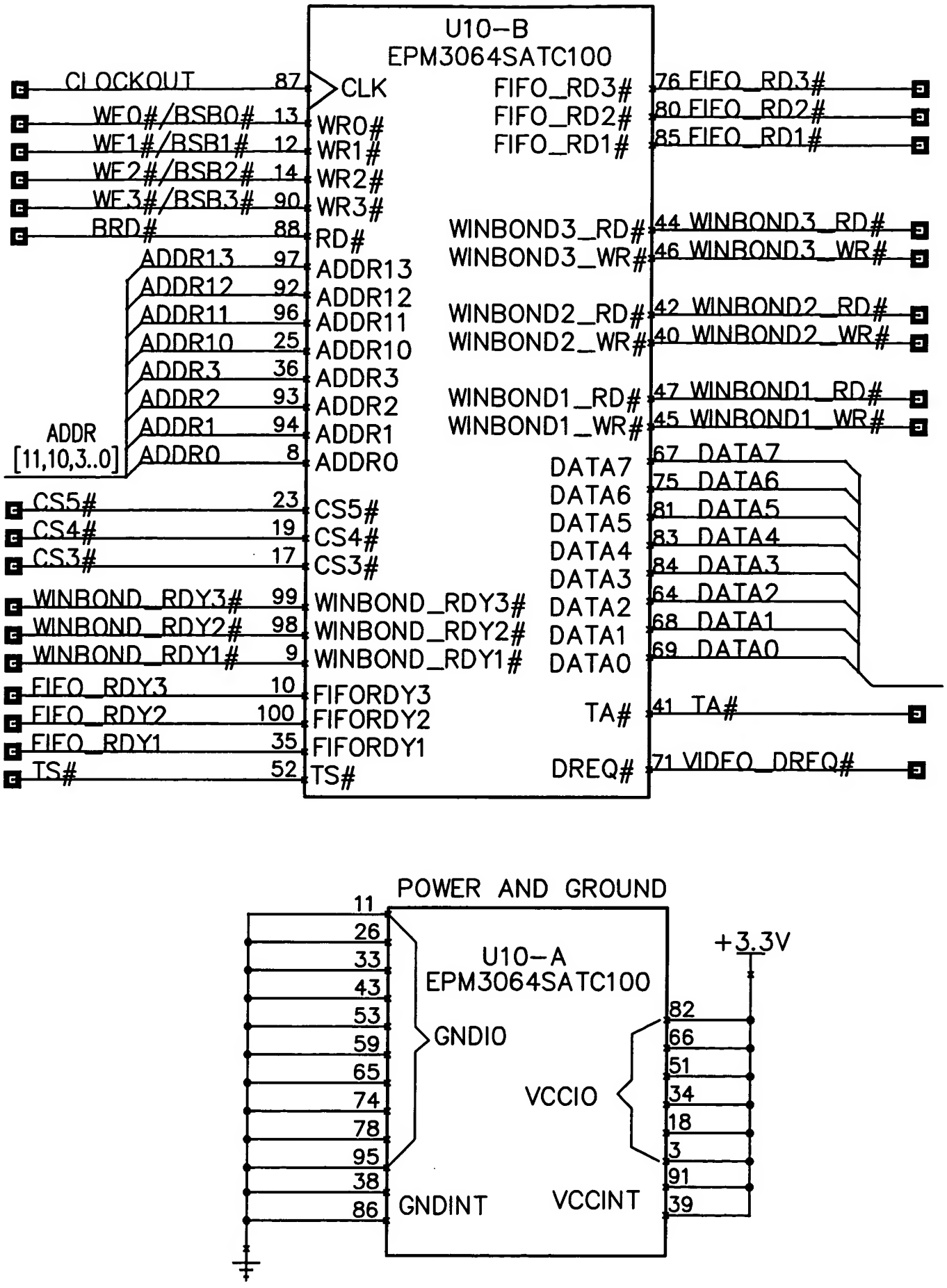
U10-B
EPM3064SATC100
CLOCKOUT 87 CLK
WE0#/BSB0# 13 WR0#
WE1#/BSB1# 12 WR1#
WE2#/BSB2# 14 WR2#
WE3#/BSB3# 90 WR3#
BRD# 88 RD#
ADDR13 97 ADDR13
ADDR12 92 ADDR12
ADDR11 96 ADDR11
ADDR10 25 ADDR10
ADDR3 36 ADDR3
ADDR2 93 ADDR2
ADDR1 94 ADDR1
ADDR0 8 ADDR0
ADDR [11,10,3..0]
CS5# 23 CS5#
CS4# 19 CS4#
CS3# 17 CS3#
WINBOND_RDY3# 99 WINBOND_RDY3#
WINBOND_RDY2# 98 WINBOND_RDY2#
WINBOND_RDY1# 9 WINBOND_RDY1#
FIFO_RDY3 10 FIFORDY3
FIFO_RDY2 100 FIFORDY2
FIFO_RDY1 35 FIFORDY1
TS# 52 TS#
FIFO_RD3# 76 FIFO_RD3#
FIFO_RD2# 80 FIFO_RD2#
FIFO_RD1# 85 FIFO_RD1#
WINBOND3_RD# 44 WINBOND3_RD#
WINBOND3_WR# 46 WINBOND3_WR#
WINBOND2_RD# 42 WINBOND2_RD#
WINBOND2_WR# 40 WINBOND2_WR#
WINBOND1_RD# 47 WINBOND1_RD#
WINBOND1_WR# 45 WINBOND1_WR#
DATA7 67 DATA7
DATA6 75 DATA6
DATA5 81 DATA5
DATA4 83 DATA4
DATA3 84 DATA3
DATA2 64 DATA2
DATA1 68 DATA1
DATA0 69 DATA0
TA# 41 TA#
DREQ# 71 VIDEO_DREQ#
POWER AND GROUND
11
26
33
43
53
59
65
74
78
95
38
86
U10-A
EPM3064SATC100
GNDIO
GNDINT
+3.3V
82
66
51
VCCIO
34
18
3
91
VCCINT
39

FIG. 160

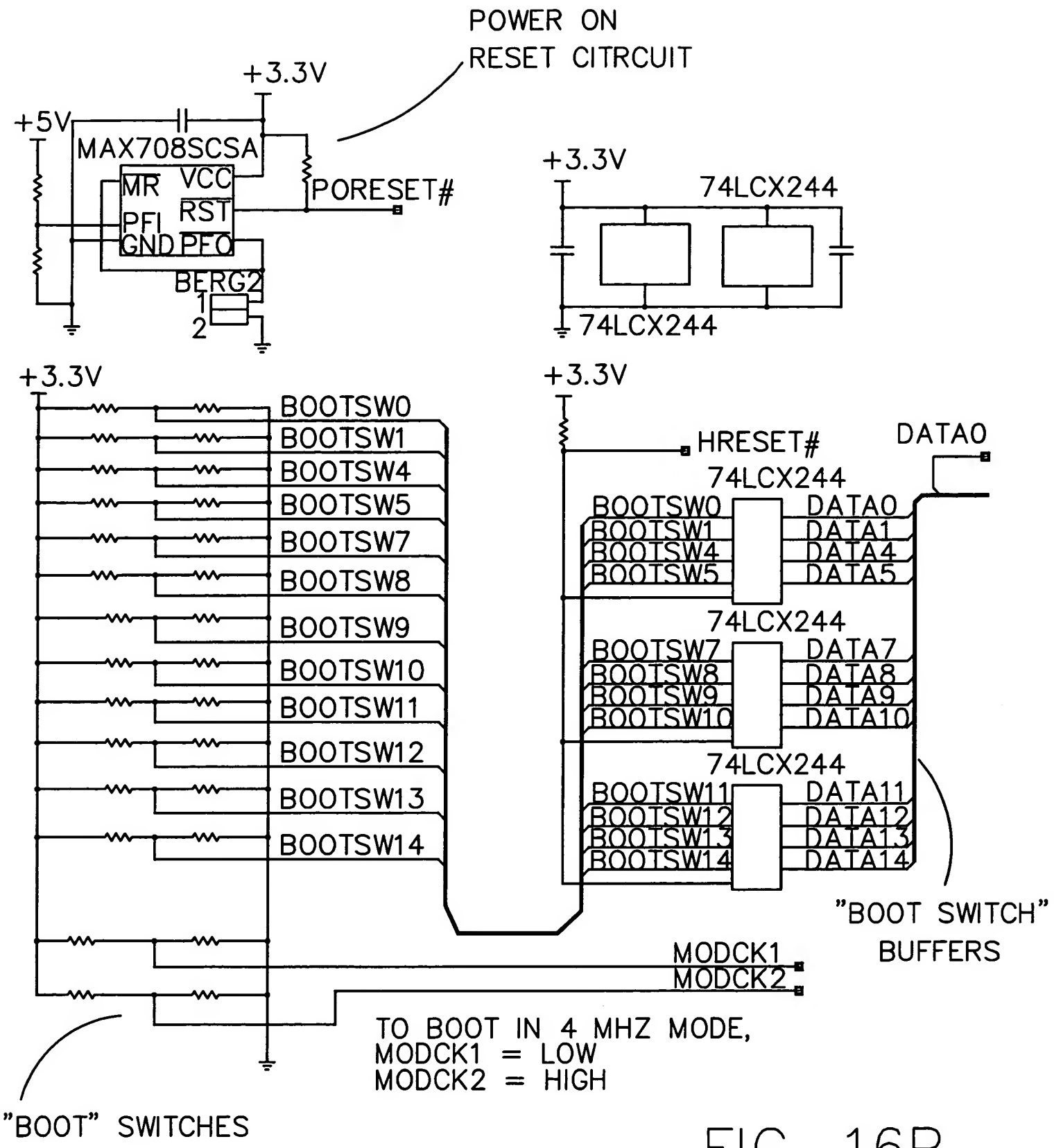
POWER ON
RESET CITRCUIT
+3.3V
+5V
MAX708SCSA
MR
VCC
RST
PFI
GND
PFO
PORESET#
BERG2
1
2
+3.3V
74LCX244
74LCX244
+3.3V
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
+3.3V
HRESET#
DATA0
74LCX244
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
DATA0
DATA1
DATA4
DATA5
74LCX244
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
DATA7
DATA8
DATA9
DATA10
74LCX244
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
DATA11
DATA12
DATA13
DATA14
"BOOT SWITCH"
BUFFERS
MODCK1
MODCK2
TO BOOT IN 4 MHZ MODE,
MODCK1 = LOW
MODCK2 = HIGH
"BOOT" SWITCHES

FIG. 16P

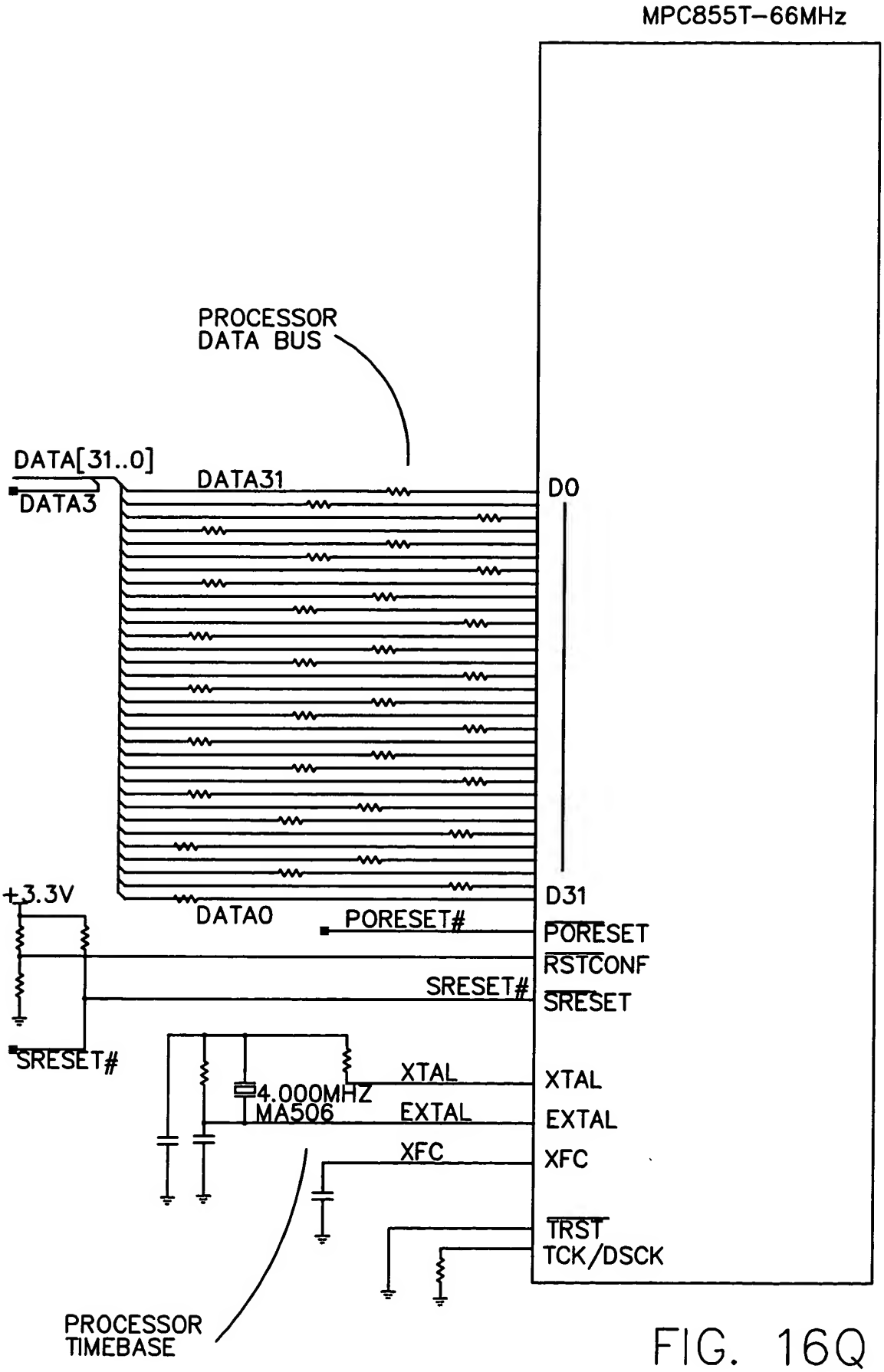
MPC855T-66MHz
PROCESSOR
DATA BUS
DATA[31..0]
DATA31
DATA3
D0
D31
DATA0
+3.3V
PORESET#
PORESET
RSTCONF
SRESET#
SRESET
SRESET#
XTAL
4.000MHZ
MA506
EXTAL
XTAL
EXTAL
XFC
XFC
TRST
TCK/DSCK
PROCESSOR
TIMEBASE

FIG. 16Q

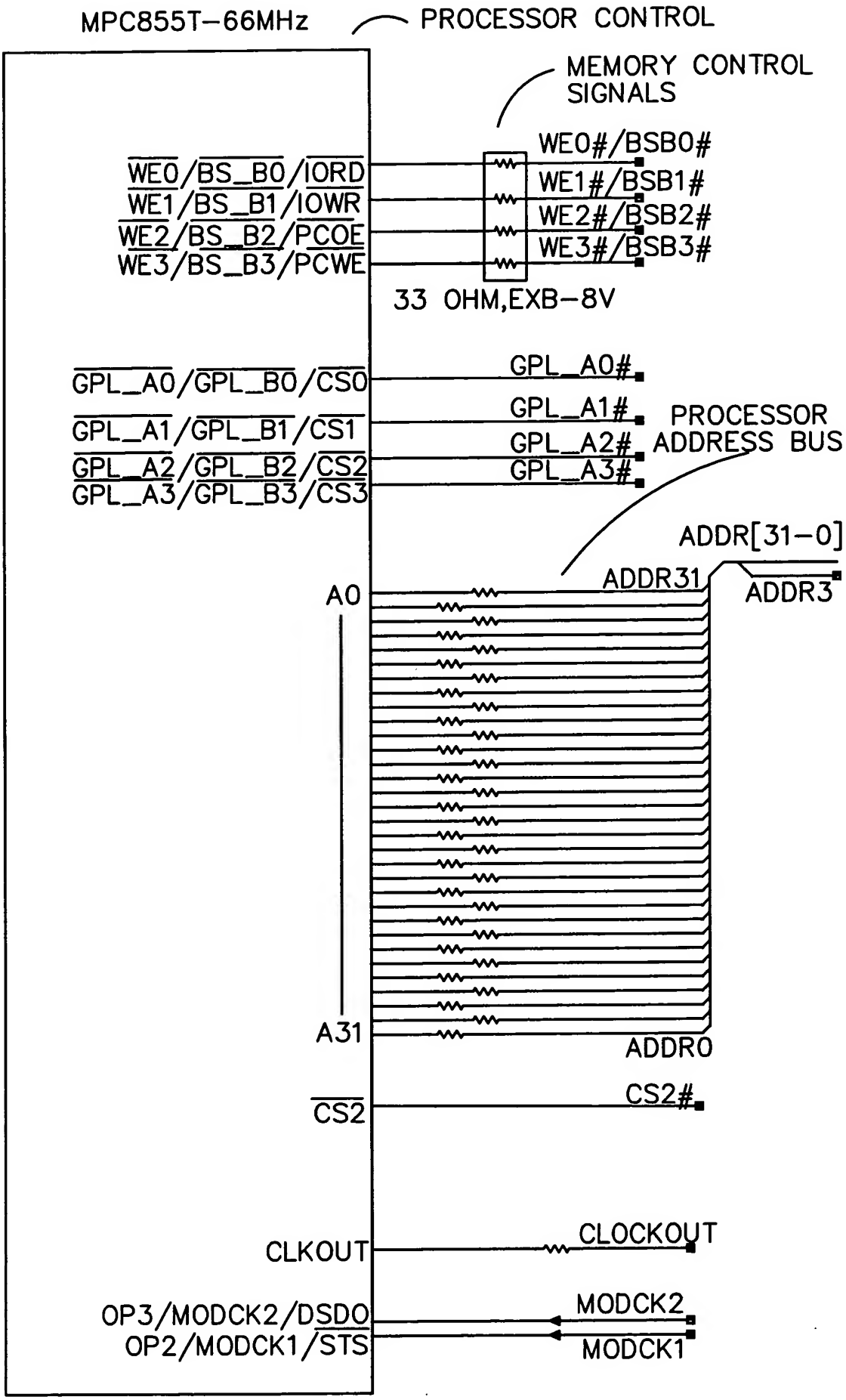
MPC855T-66MHz
PROCESSOR CONTROL
MEMORY CONTROL SIGNALS
WE0/BS_B0/IORD
WE1/BS_B1/IOWR
WE2/BS_B2/PCOE
WE3/BS_B3/PCWE
WE0#/BSB0#
WE1#/BSB1#
WE2#/BSB2#
WE3#/BSB3#
33 OHM,EXB-8V
GPL_A0/GPL_B0/CS0
GPL_A1/GPL_B1/CS1
GPL_A2/GPL_B2/CS2
GPL_A3/GPL_B3/CS3
GPL_A0#
GPL_A1#
GPL_A2#
GPL_A3#
PROCESSOR ADDRESS BUS
ADDR[31-0]
ADDR31
ADDR3
A0
A31
ADDR0
CS2
CS2#
CLKOUT
CLOCKOUT
OP3/MODCK2/DSDO
OP2/MODCK1/STS
MODCK2
MODCK1

FIG. 16R

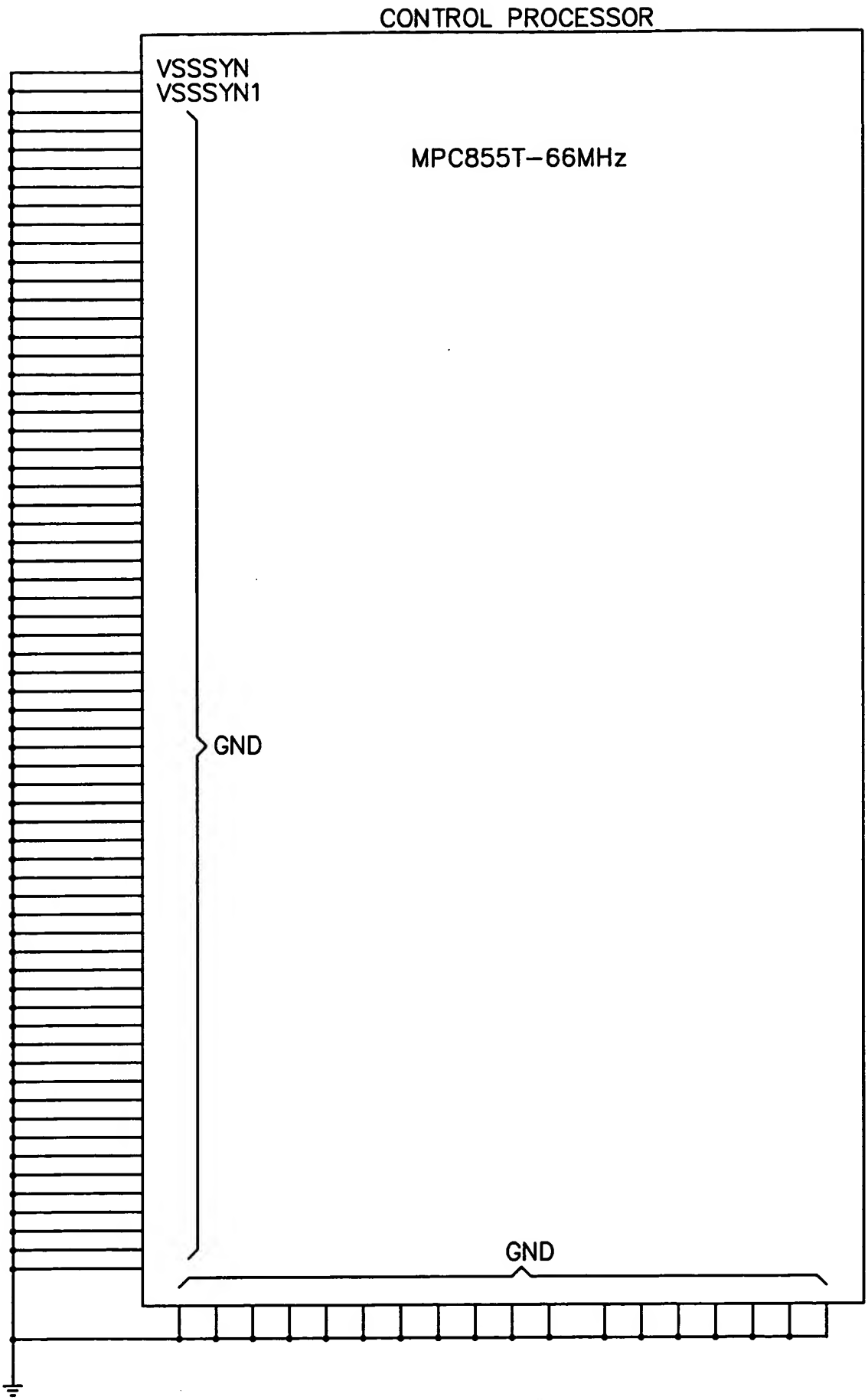

FIG. 16S

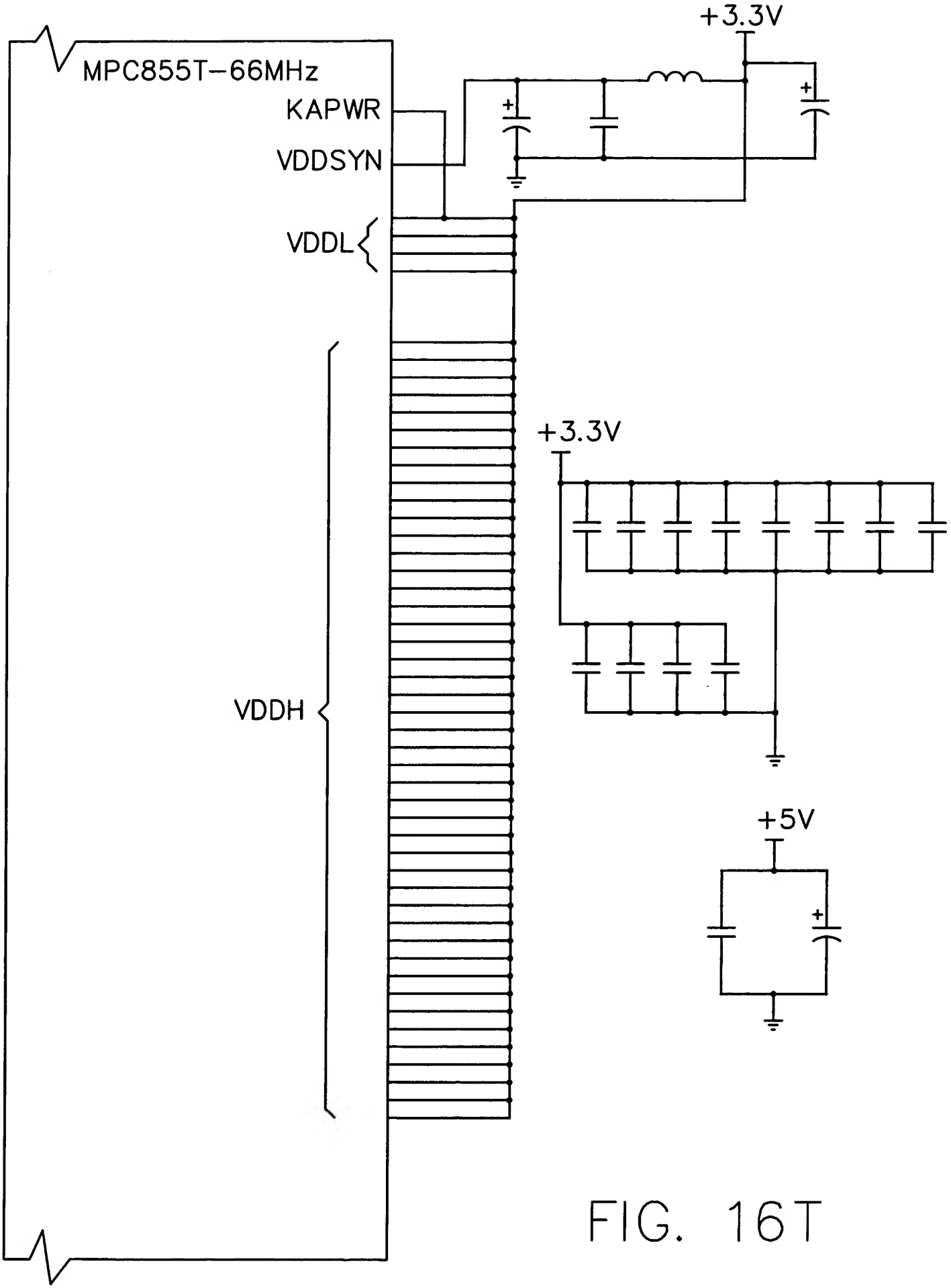

FIG. 16T

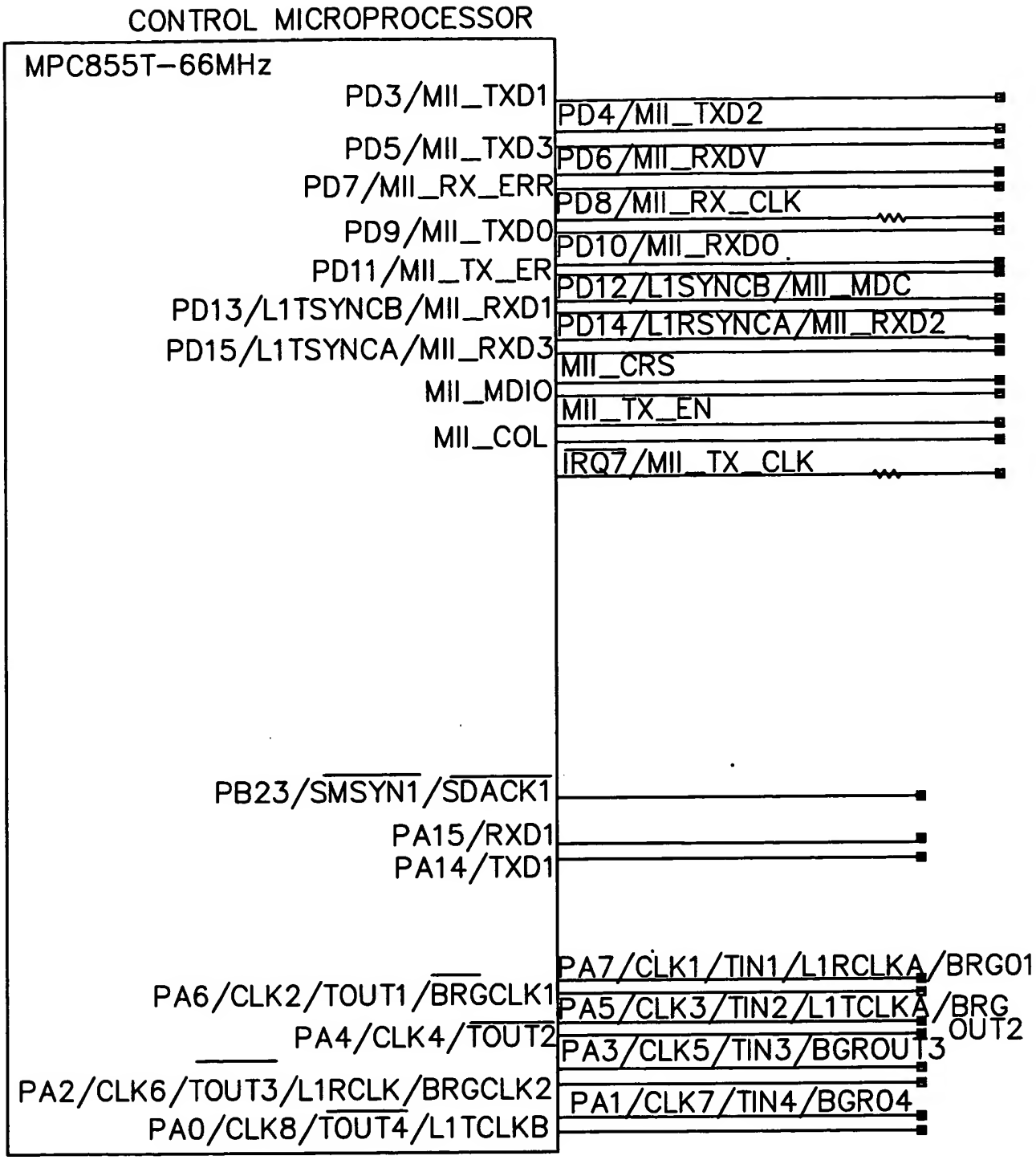
CONTROL MICROPROCESSOR
MPC855T-66MHz
PD3/MII_TXD1
PD4/MII_TXD2
PD5/MII_TXD3
PD6/MII_RXDV
PD7/MII_RX_ERR
PD8/MII_RX_CLK
PD9/MII_TXD0
PD10/MII_RXD0
PD11/MII_TX_ER
PD12/L1SYNCB/MII_MDC
PD13/L1TSYNCB/MII_RXD1
PD14/L1RSYNCA/MII_RXD2
PD15/L1TSYNCA/MII_RXD3
MII_CRS
MII_MDIO
MII_TX_EN
MII_COL
IRQ7/MII_TX_CLK
PB23/SMSYN1/SDACK1
PA15/RXD1
PA14/TXD1
PA7/CLK1/TIN1/L1RCLKA/BRG01
PA6/CLK2/TOUT1/BRGCLK1
PA5/CLK3/TIN2/L1TCLKA/BRG OUT2
PA4/CLK4/TOUT2
PA3/CLK5/TIN3/BGROUT3
PA2/CLK6/TOUT3/L1RCLK/BRGCLK2
PA1/CLK7/TIN4/BGR04
PA0/CLK8/TOUT4/L1TCLKB

FIG. 16U

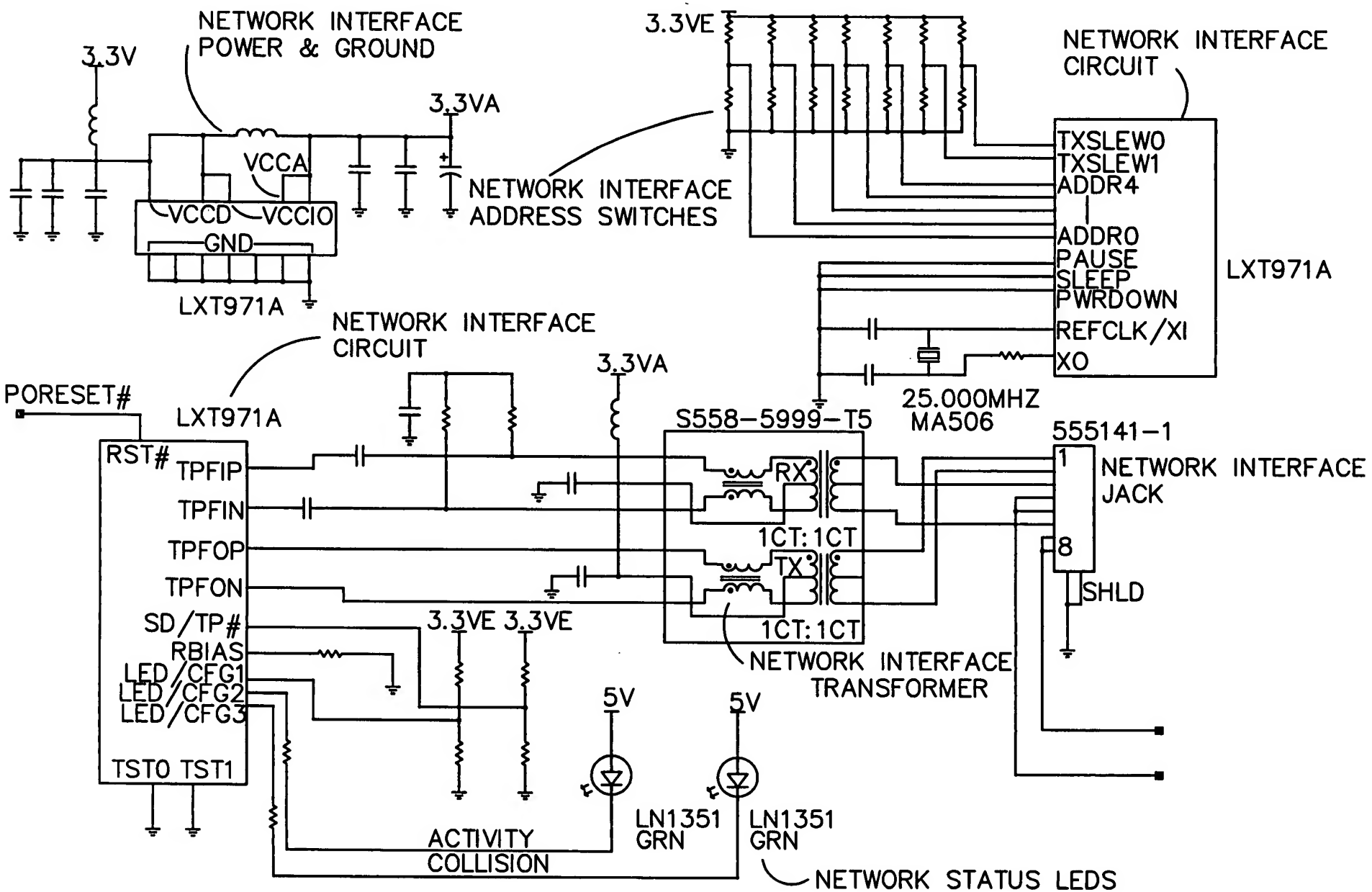
NETWORK INTERFACE
POWER & GROUND
3.3V
3.3VA
VCCA
VCCD
VCCIO
GND
LXT971A
NETWORK INTERFACE
ADDRESS SWITCHES
3.3VE
NETWORK INTERFACE
CIRCUIT
TXSLEW0
TXSLEW1
ADDR4
ADDR0
PAUSE
SLEEP
PWRDOWN
REFCLK/XI
XO
LXT971A
25.000MHZ
MA506
NETWORK INTERFACE
CIRCUIT
LXT971A
PORESET#
RST#
TPFIP
TPFIN
TPFOP
TPFON
SD/TP#
RBIAS
LED/CFG1
LED/CFG2
LED/CFG3
TST0 TST1
3.3VA
S558-5999-T5
RX
1CT:1CT
TX
1CT:1CT
NETWORK INTERFACE
TRANSFORMER
555141-1
1
8
SHLD
NETWORK INTERFACE
JACK
3.3VE 3.3VE
5V
5V
LN1351
GRN
LN1351
GRN
ACTIVITY
COLLISION
NETWORK STATUS LEDS

FIG. 16V

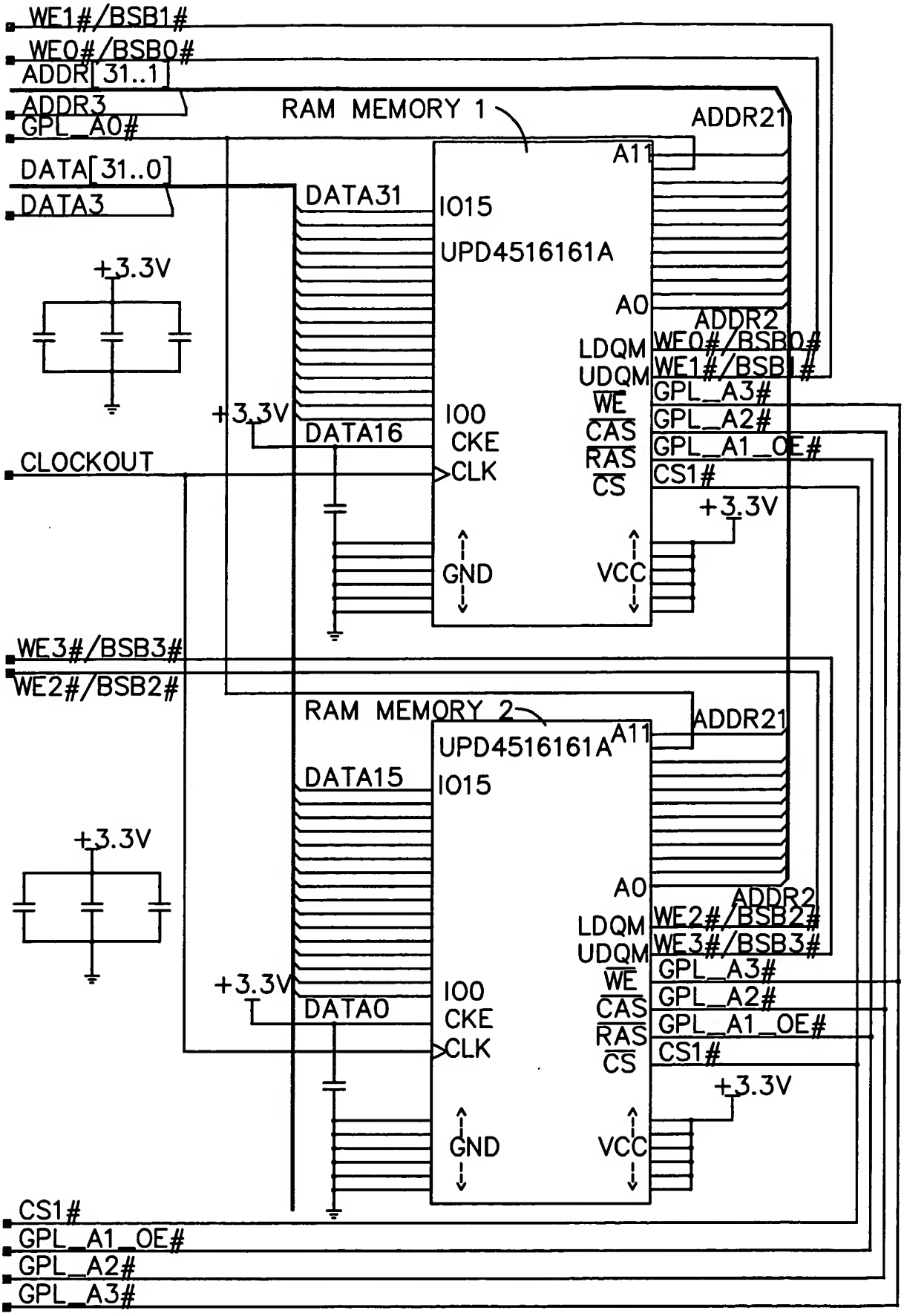
WE1#/BSB1#
WE0#/BSB0#
ADDR[31..1]
ADDR3
GPL_A0#
DATA[31..0]
DATA3
RAM MEMORY 1
ADDR21
A11
DATA31
IO15
UPD4516161A
A0
ADDR2
LDQM
WE0#/BSB0#
UDQM
WE1#/BSB1#
WE
GPL_A3#
CAS
GPL_A2#
RAS
GPL_A1_OE#
CS
CS1#
+3.3V
IO0
DATA16
CKE
CLOCKOUT
CLK
GND
VCC
WE3#/BSB3#
WE2#/BSB2#
RAM MEMORY 2
ADDR21
UPD4516161A
A11
DATA15
IO15
A0
ADDR2
LDQM
WE2#/BSB2#
UDQM
WE3#/BSB3#
WE
GPL_A3#
CAS
GPL_A2#
RAS
GPL_A1_OE#
CS
CS1#
+3.3V
IO0
DATA0
CKE
CLK
GND
VCC
CS1#
GPL_A1_OE#
GPL_A2#
GPL_A3#

FIG. 16W

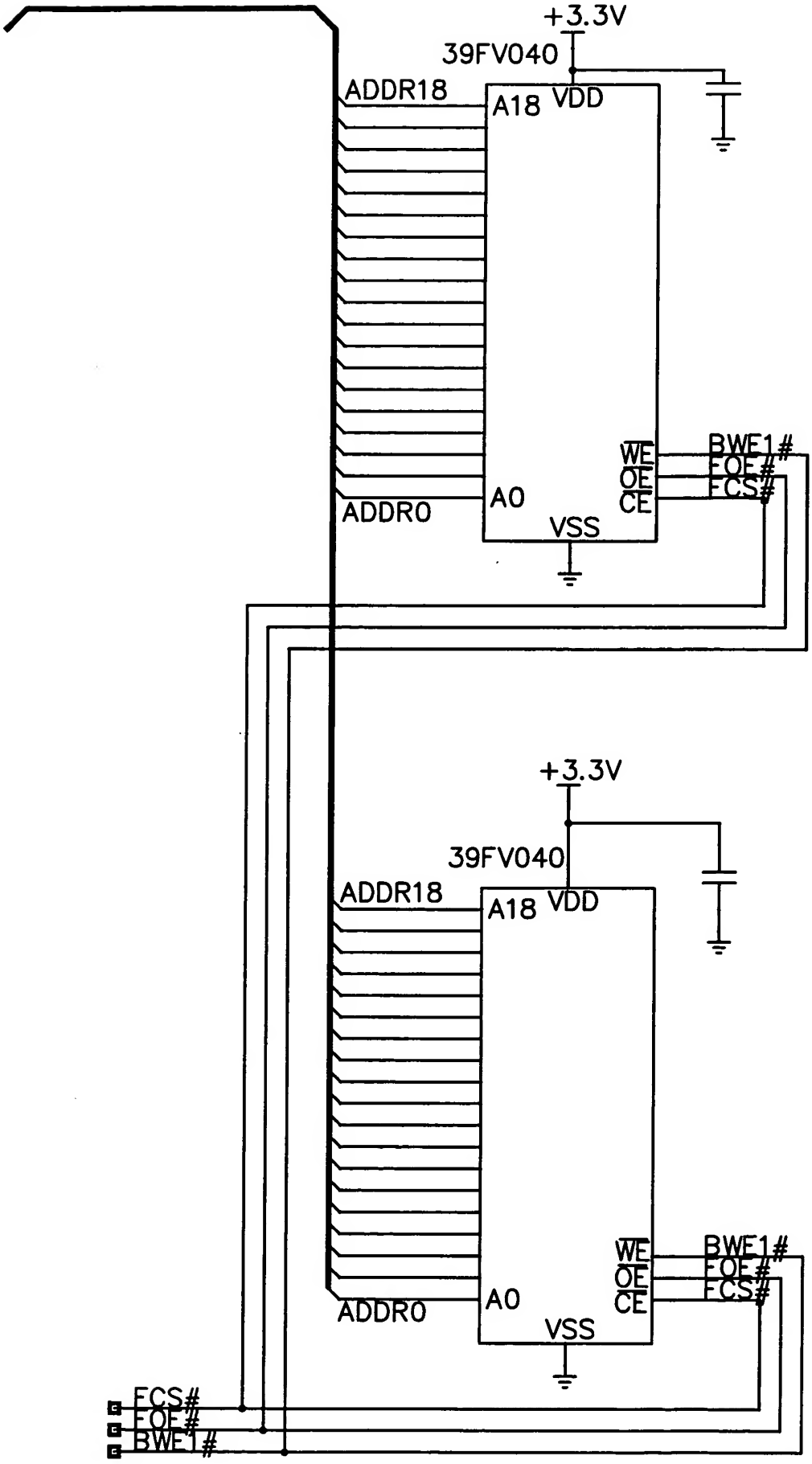
+3.3V
39FV040
ADDR18
A18
VDD
WE
OE
CE
BWE1#
FOE#
FCS#
ADDR0
A0
VSS
+3.3V
39FV040
ADDR18
A18
VDD
WE
OE
CE
BWE1#
FOE#
FCS#
ADDR0
A0
VSS
FCS#
FOE#
BWE1#

FIG. 16X

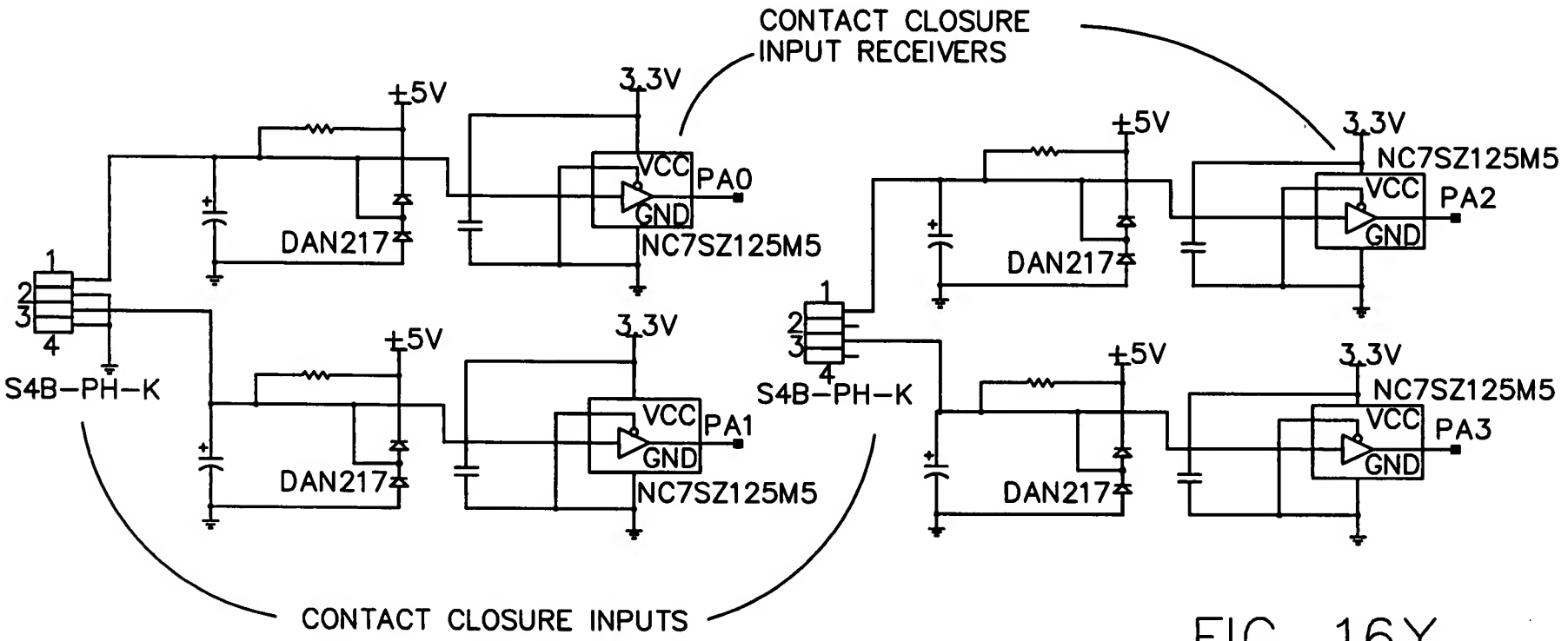
CONTACT CLOSURE
INPUT RECEIVERS
+5V
3.3V
VCC
PA0
GND
NC7SZ125M5
DAN217
1
2
3
4
S4B-PH-K
PA1
PA2
PA3
CONTACT CLOSURE INPUTS

FIG. 16Y

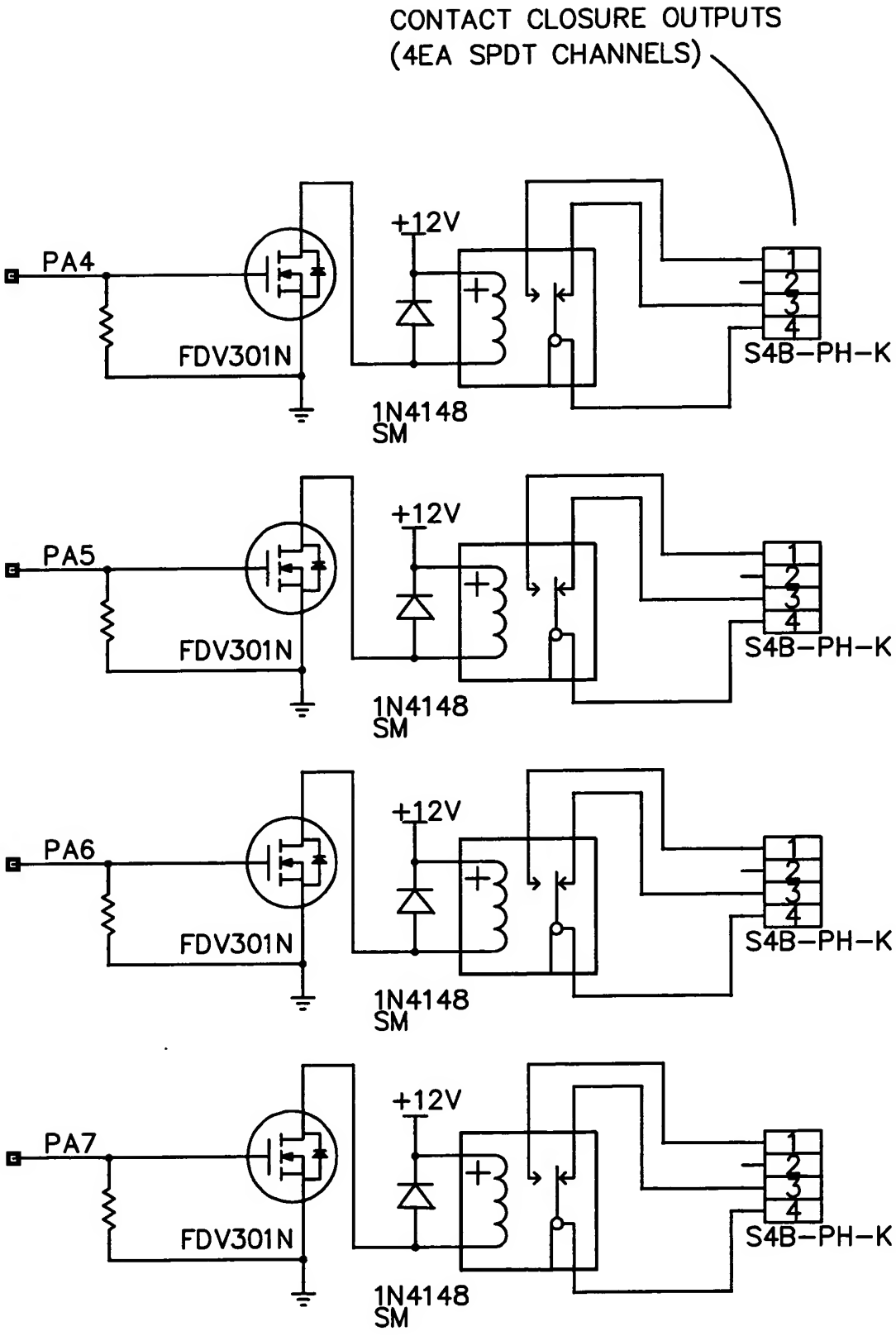
CONTACT CLOSURE OUTPUTS
(4EA SPDT CHANNELS)
PA4
FDV301N
+12V
1N4148
SM
S4B-PH-K
PA5
FDV301N
+12V
1N4148
SM
S4B-PH-K
PA6
FDV301N
+12V
1N4148
SM
S4B-PH-K
PA7
FDV301N
+12V
1N4148
SM
S4B-PH-K

FIG. 16Z

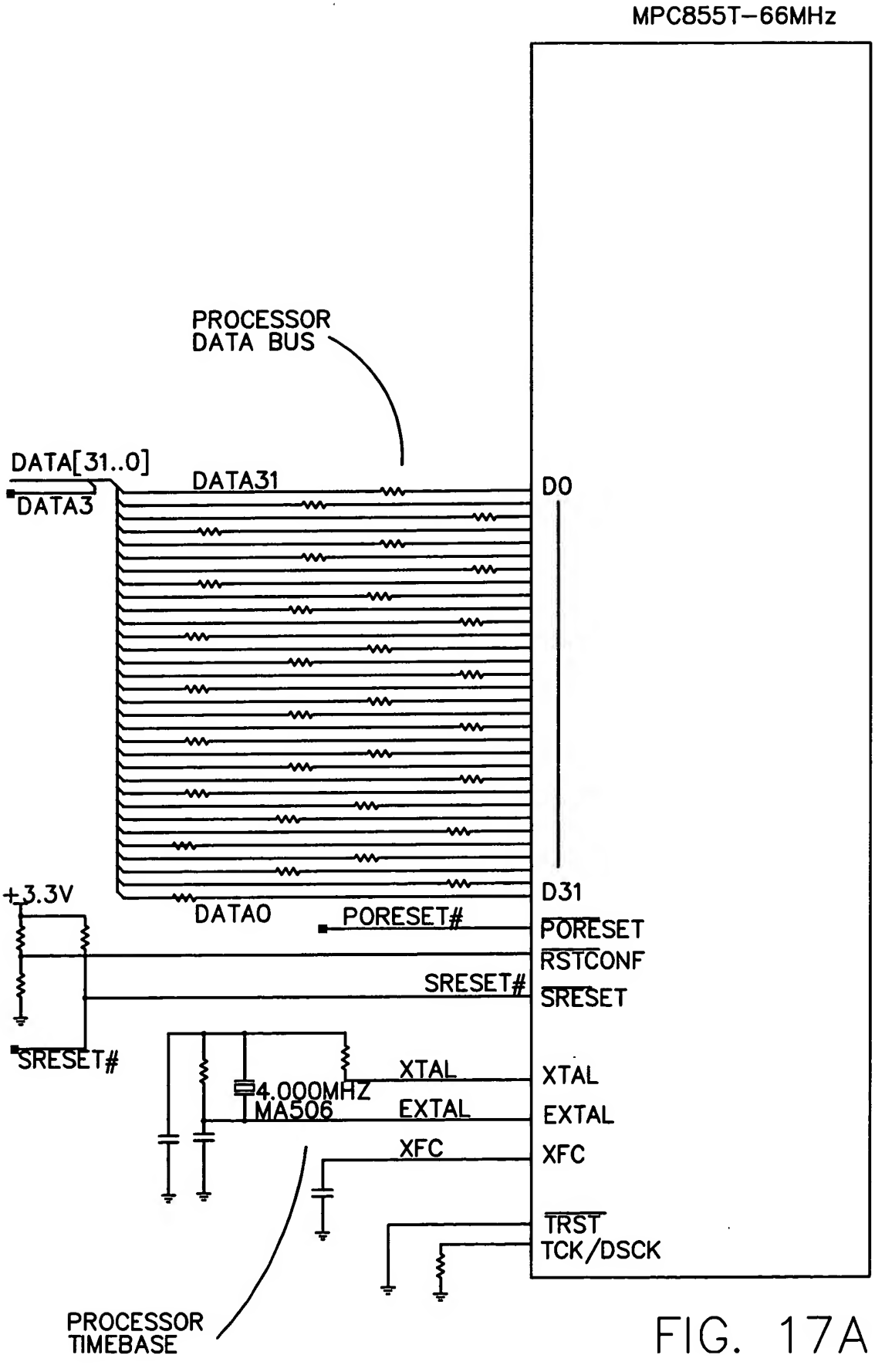
MPC855T–66MHz
PROCESSOR
DATA BUS
DATA[31..0]
DATA31
DATA3
D0
D31
DATA0
+3.3V
PORESET#
PORESET
RSTCONF
SRESET#
SRESET
SRESET#
XTAL
4.000MHZ
MA506
EXTAL
XFC
TRST
TCK/DSCK
PROCESSOR
TIMEBASE

FIG. 17A

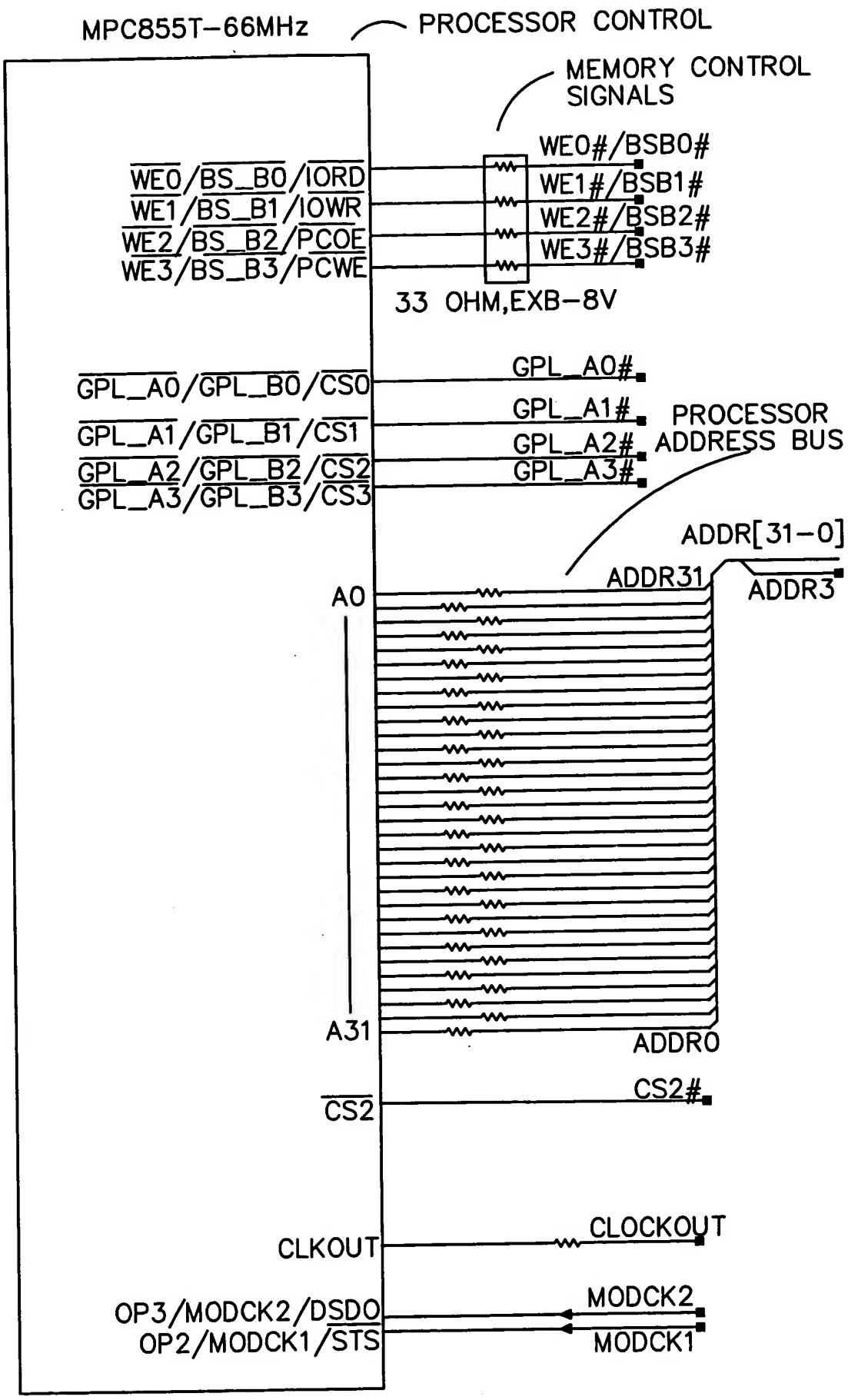
MPC855T-66MHz
PROCESSOR CONTROL
MEMORY CONTROL SIGNALS
WE0/BS_B0/IORD
WE1/BS_B1/IOWR
WE2/BS_B2/PCOE
WE3/BS_B3/PCWE
WE0#/BSB0#
WE1#/BSB1#
WE2#/BSB2#
WE3#/BSB3#
33 OHM,EXB-8V
GPL_A0/GPL_B0/CS0
GPL_A1/GPL_B1/CS1
GPL_A2/GPL_B2/CS2
GPL_A3/GPL_B3/CS3
GPL_A0#
GPL_A1#
GPL_A2#
GPL_A3#
PROCESSOR ADDRESS BUS
ADDR[31-0]
ADDR31
ADDR3
A0
A31
ADDR0
CS2
CS2#
CLKOUT
CLOCKOUT
OP3/MODCK2/DSDO
OP2/MODCK1/STS
MODCK2
MODCK1

FIG. 17B

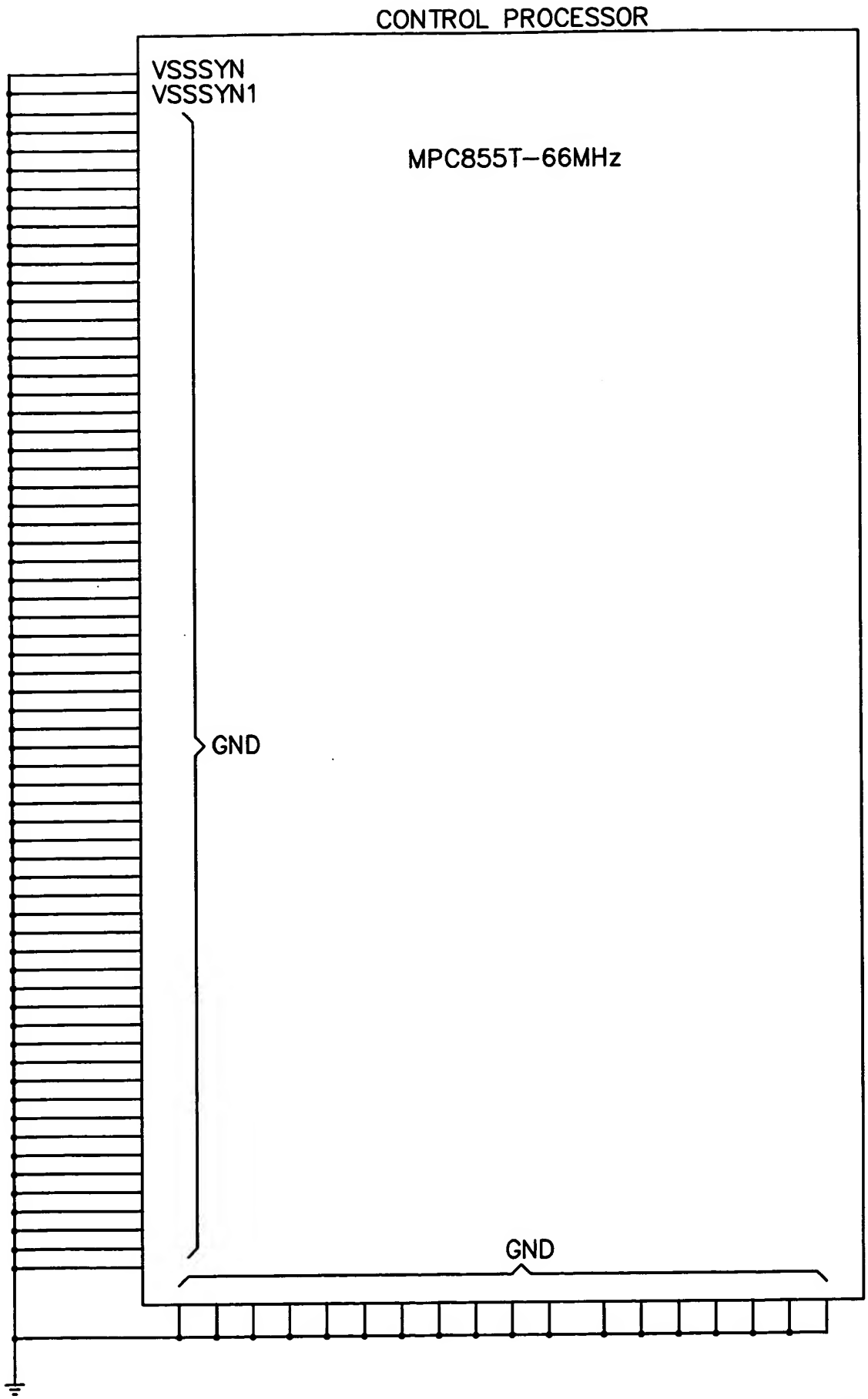

FIG. 17C

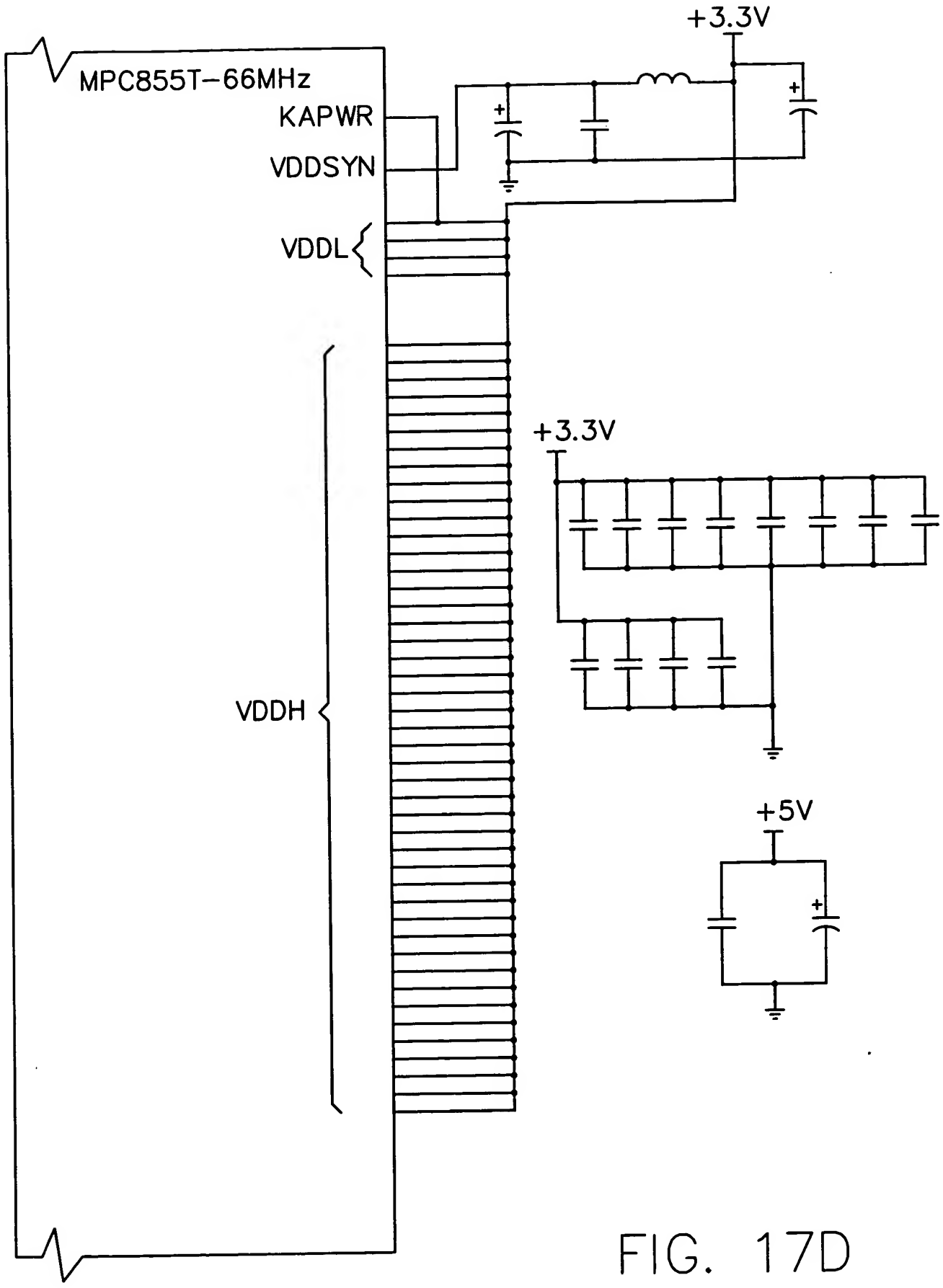

FIG. 17D

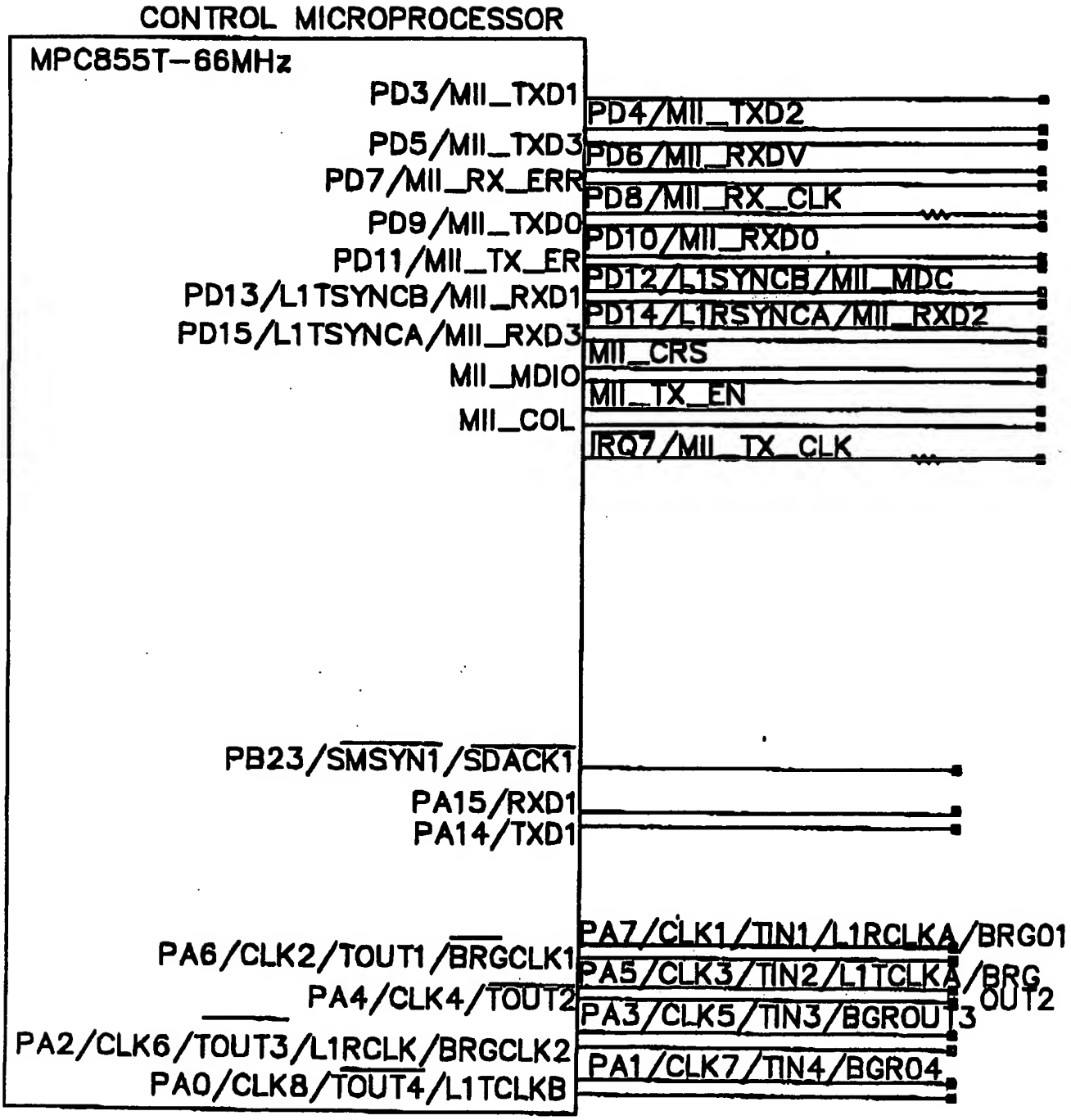
CONTROL MICROPROCESSOR
MPC855T–66MHz
PD3/MII_TXD1
PD4/MII_TXD2
PD5/MII_TXD3
PD6/MII_RXDV
PD7/MII_RX_ERR
PD8/MII_RX_CLK
PD9/MII_TXD0
PD10/MII_RXD0
PD11/MII_TX_ER
PD12/L1SYNCB/MII_MDC
PD13/L1TSYNCB/MII_RXD1
PD14/L1RSYNCA/MII_RXD2
PD15/L1TSYNCA/MII_RXD3
MII_CRS
MII_MDIO
MII_TX_EN
MII_COL
IRQ7/MII_TX_CLK
PB23/SMSYN1/SDACK1
PA15/RXD1
PA14/TXD1
PA7/CLK1/TIN1/L1RCLKA/BRG01
PA6/CLK2/TOUT1/BRGCLK1
PA5/CLK3/TIN2/L1TCLKA/BRG
PA4/CLK4/TOUT2
OUT2
PA3/CLK5/TIN3/BGROUT3
PA2/CLK6/TOUT3/L1RCLK/BRGCLK2
PA1/CLK7/TIN4/BGR04
PA0/CLK8/TOUT4/L1TCLKB

FIG. 17E

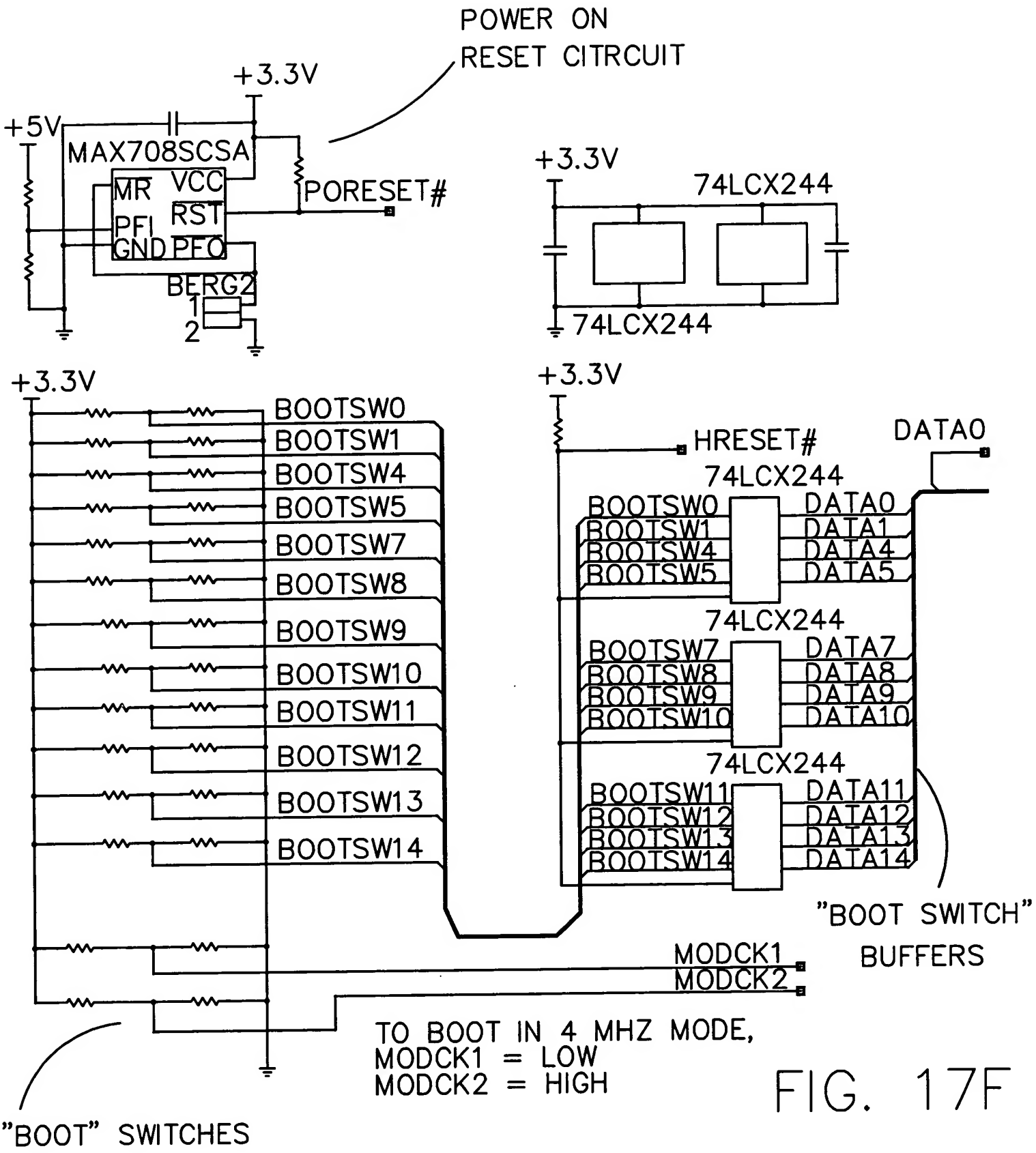
POWER ON
RESET CITRCUIT
+3.3V
+5V
MAX708SCSA
MR
VCC
RST
PFI
GND
PFO
PORESET#
BERG2
1
2
+3.3V
74LCX244
74LCX244
+3.3V
+3.3V
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
HRESET#
DATA0
74LCX244
BOOTSW0
BOOTSW1
BOOTSW4
BOOTSW5
DATA0
DATA1
DATA4
DATA5
74LCX244
BOOTSW7
BOOTSW8
BOOTSW9
BOOTSW10
DATA7
DATA8
DATA9
DATA10
74LCX244
BOOTSW11
BOOTSW12
BOOTSW13
BOOTSW14
DATA11
DATA12
DATA13
DATA14
"BOOT SWITCH"
BUFFERS
MODCK1
MODCK2
TO BOOT IN 4 MHZ MODE,
MODCK1 = LOW
MODCK2 = HIGH
"BOOT" SWITCHES

FIG. 17F

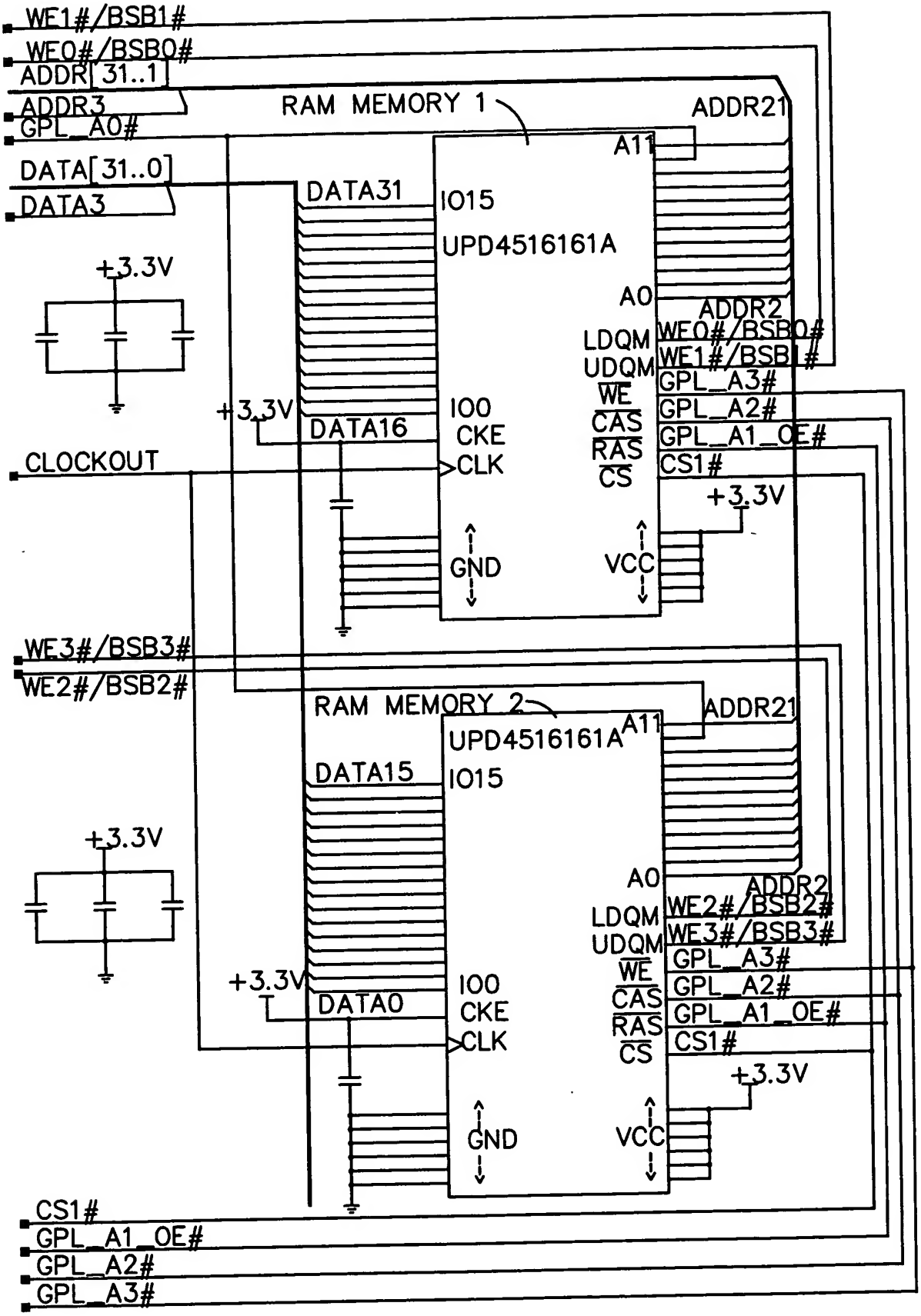
WE1#/BSB1#
WE0#/BSB0#
ADDR[31..1]
ADDR3
GPL_A0#
DATA[31..0]
DATA3
RAM MEMORY 1
ADDR21
A11
DATA31
IO15
UPD4516161A
+3.3V
A0
ADDR2
LDQM
WE0#/BSB0#
UDQM
WE1#/BSB1#
WE
GPL_A3#
+3.3V
IO0
CAS
GPL_A2#
DATA16
CKE
RAS
GPL_A1_OE#
CLOCKOUT
CLK
CS
CS1#
+3.3V
GND
VCC
WE3#/BSB3#
WE2#/BSB2#
RAM MEMORY 2
ADDR21
UPD4516161A
A11
DATA15
IO15
+3.3V
A0
ADDR2
LDQM
WE2#/BSB2#
UDQM
WE3#/BSB3#
WE
GPL_A3#
+3.3V
IO0
CAS
GPL_A2#
DATA0
CKE
RAS
GPL_A1_OE#
CLK
CS
CS1#
+3.3V
GND
VCC
CS1#
GPL_A1_OE#
GPL_A2#
GPL_A3#

FIG. 17G

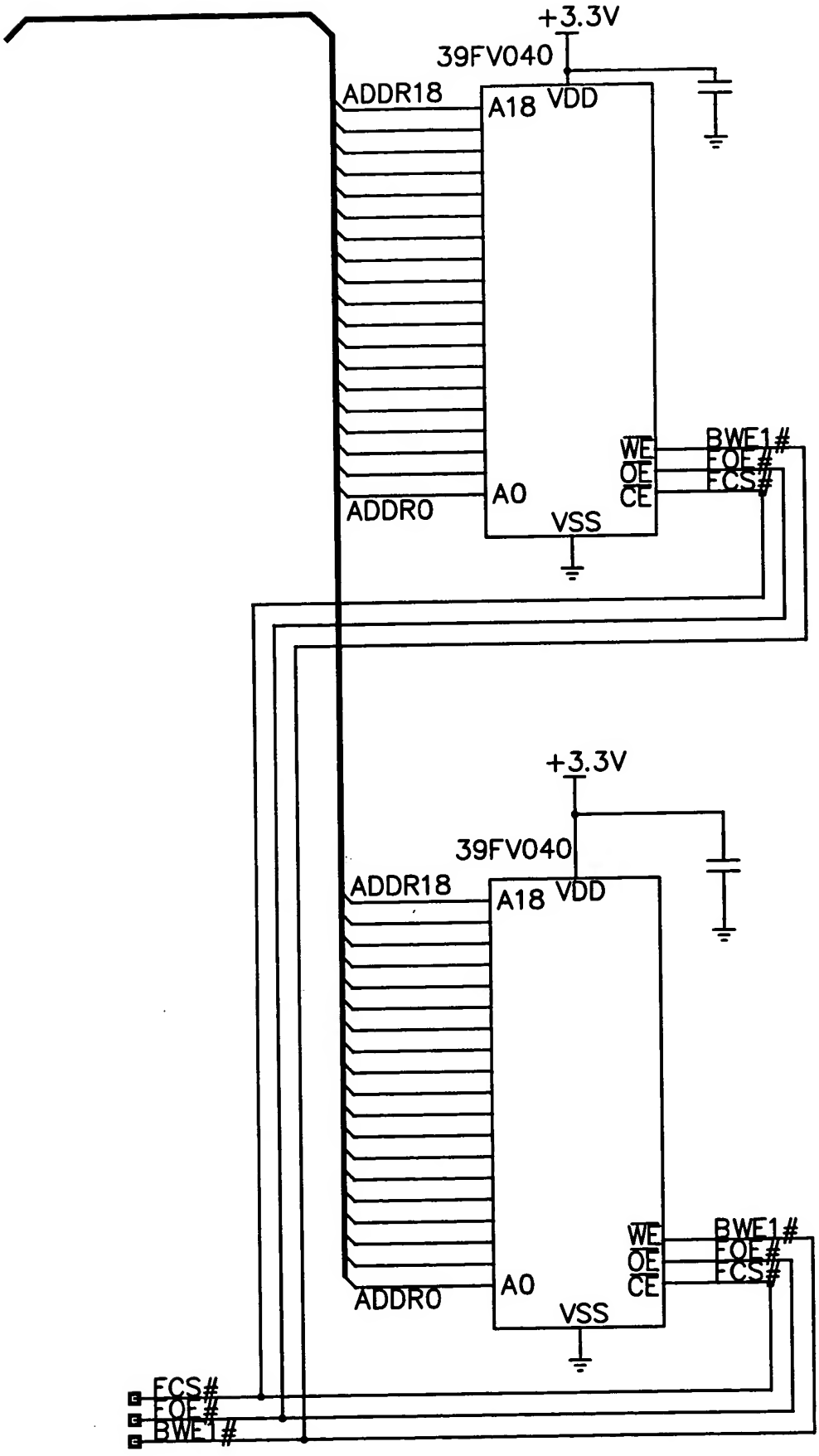
+3.3V
39FV040
ADDR18
A18
VDD
WE
OE
CE
BWE1#
FOE#
FCS#
ADDR0
A0
VSS
+3.3V
39FV040
ADDR18
A18
VDD
WE
OE
CE
BWE1#
FOE#
FCS#
ADDR0
A0
VSS
FCS#
FOE#
BWE1#

FIG. 17H

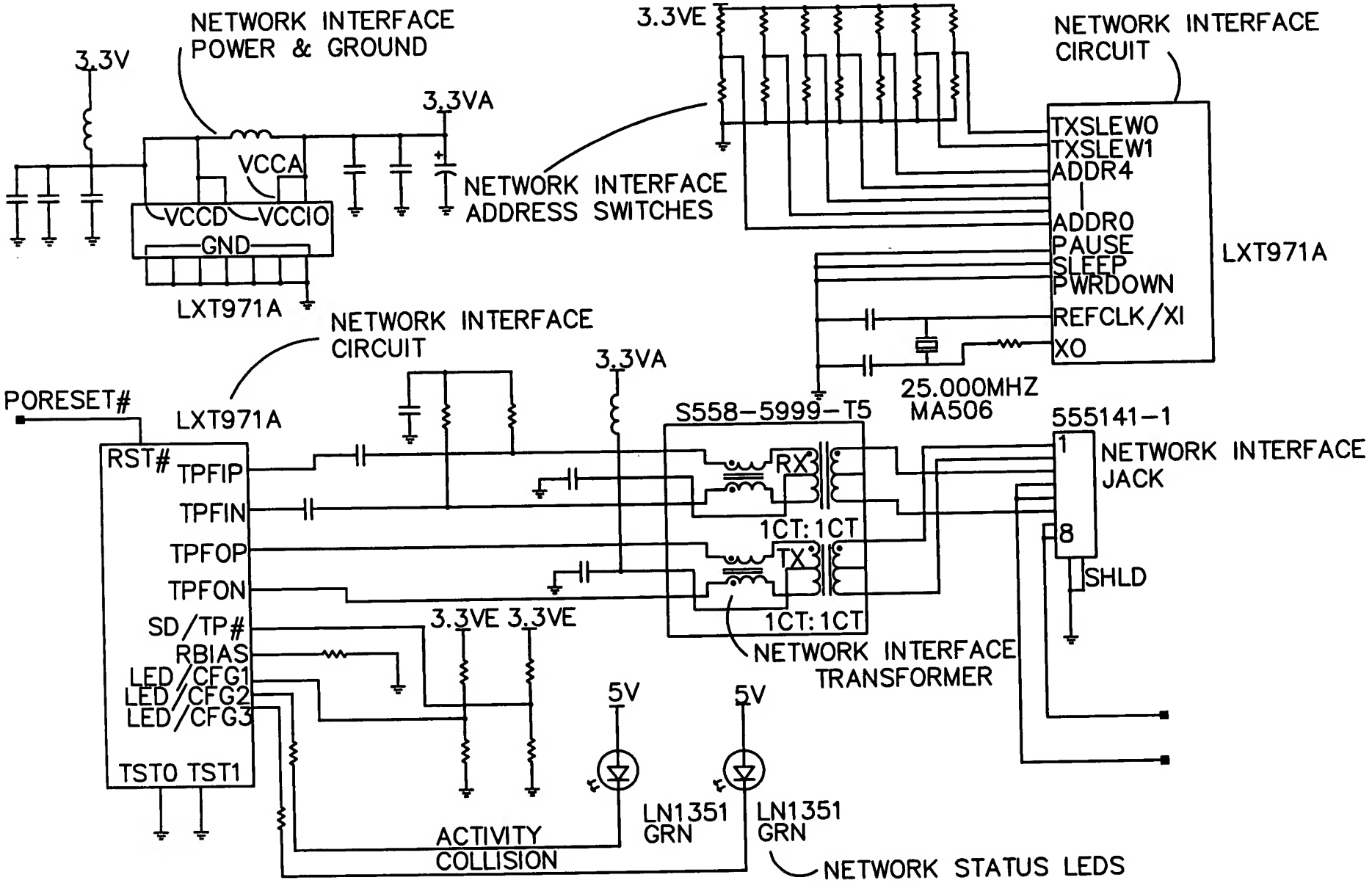
NETWORK INTERFACE
POWER & GROUND
3.3V
3.3VA
VCCA
VCCD
VCCIO
GND
LXT971A
NETWORK INTERFACE
ADDRESS SWITCHES
3.3VE
NETWORK INTERFACE
CIRCUIT
TXSLEW0
TXSLEW1
ADDR4
ADDR0
PAUSE
SLEEP
PWRDOWN
REFCLK/XI
XO
LXT971A
25.000MHZ
MA506
NETWORK INTERFACE
CIRCUIT
LXT971A
3.3VA
PORESET#
RST#
TPFIP
TPFIN
TPFOP
TPFON
SD/TP#
RBIAS
LED/CFG1
LED/CFG2
LED/CFG3
TST0 TST1
S558-5999-T5
RX
1CT:1CT
TX
1CT:1CT
NETWORK INTERFACE
TRANSFORMER
555141-1
1
8
SHLD
NETWORK INTERFACE
JACK
3.3VE 3.3VE
5V
5V
LN1351
GRN
LN1351
GRN
ACTIVITY
COLLISION
NETWORK STATUS LEDS

FIG. 17I

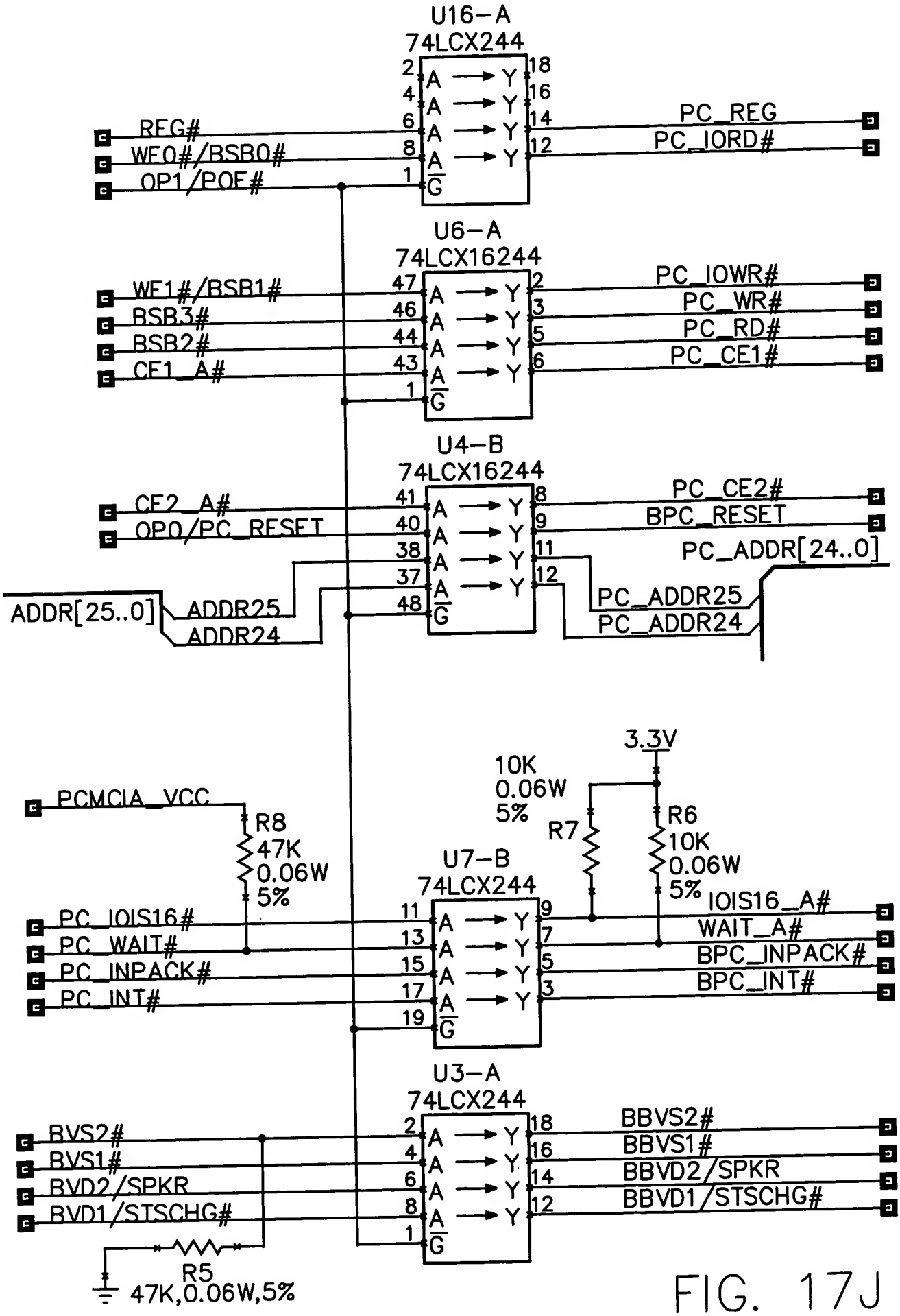
U16-A
74LCX244
REG#
WE0#/BSB0#
OP1/POE#
PC_REG
PC_IORD#
U6-A
74LCX16244
WE1#/BSB1#
BSB3#
BSB2#
CE1_A#
PC_IOWR#
PC_WR#
PC_RD#
PC_CE1#
U4-B
74LCX16244
CE2_A#
OP0/PC_RESET
ADDR[25..0]
ADDR25
ADDR24
PC_CE2#
BPC_RESET
PC_ADDR[24..0]
PC_ADDR25
PC_ADDR24
3.3V
10K
0.06W
5%
R7
R6
10K
0.06W
5%
PCMCIA_VCC
R8
47K
0.06W
5%
U7-B
74LCX244
PC_IOIS16#
PC_WAIT#
PC_INPACK#
PC_INT#
IOIS16_A#
WAIT_A#
BPC_INPACK#
BPC_INT#
U3-A
74LCX244
BVS2#
BVS1#
BVD2/SPKR
BVD1/STSCHG#
BBVS2#
BBVS1#
BBVD2/SPKR
BBVD1/STSCHG#
R5
47K,0.06W,5%

FIG. 17J

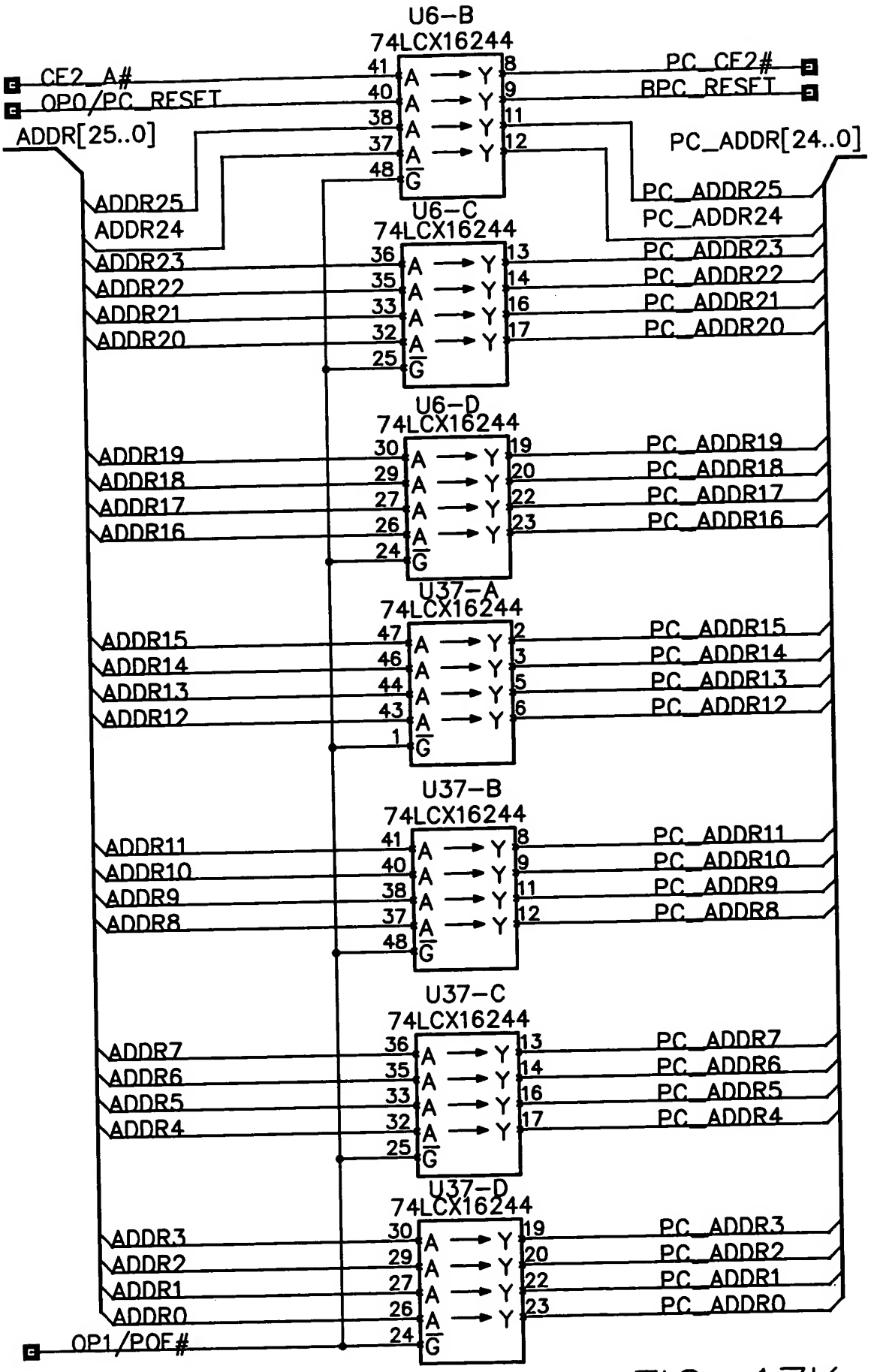
U6-B
74LCX16244
CE2_A#
OP0/PC_RESET
ADDR[25..0]
PC_CE2#
BPC_RESET
PC_ADDR[24..0]
ADDR25
ADDR24
ADDR23
ADDR22
ADDR21
ADDR20
PC_ADDR25
PC_ADDR24
PC_ADDR23
PC_ADDR22
PC_ADDR21
PC_ADDR20
U6-C
74LCX16244
U6-D
74LCX16244
ADDR19
ADDR18
ADDR17
ADDR16
PC_ADDR19
PC_ADDR18
PC_ADDR17
PC_ADDR16
U37-A
74LCX16244
ADDR15
ADDR14
ADDR13
ADDR12
PC_ADDR15
PC_ADDR14
PC_ADDR13
PC_ADDR12
U37-B
74LCX16244
ADDR11
ADDR10
ADDR9
ADDR8
PC_ADDR11
PC_ADDR10
PC_ADDR9
PC_ADDR8
U37-C
74LCX16244
ADDR7
ADDR6
ADDR5
ADDR4
PC_ADDR7
PC_ADDR6
PC_ADDR5
PC_ADDR4
U37-D
74LCX16244
ADDR3
ADDR2
ADDR1
ADDR0
OP1/POE#
PC_ADDR3
PC_ADDR2
PC_ADDR1
PC_ADDR0

FIG. 17K

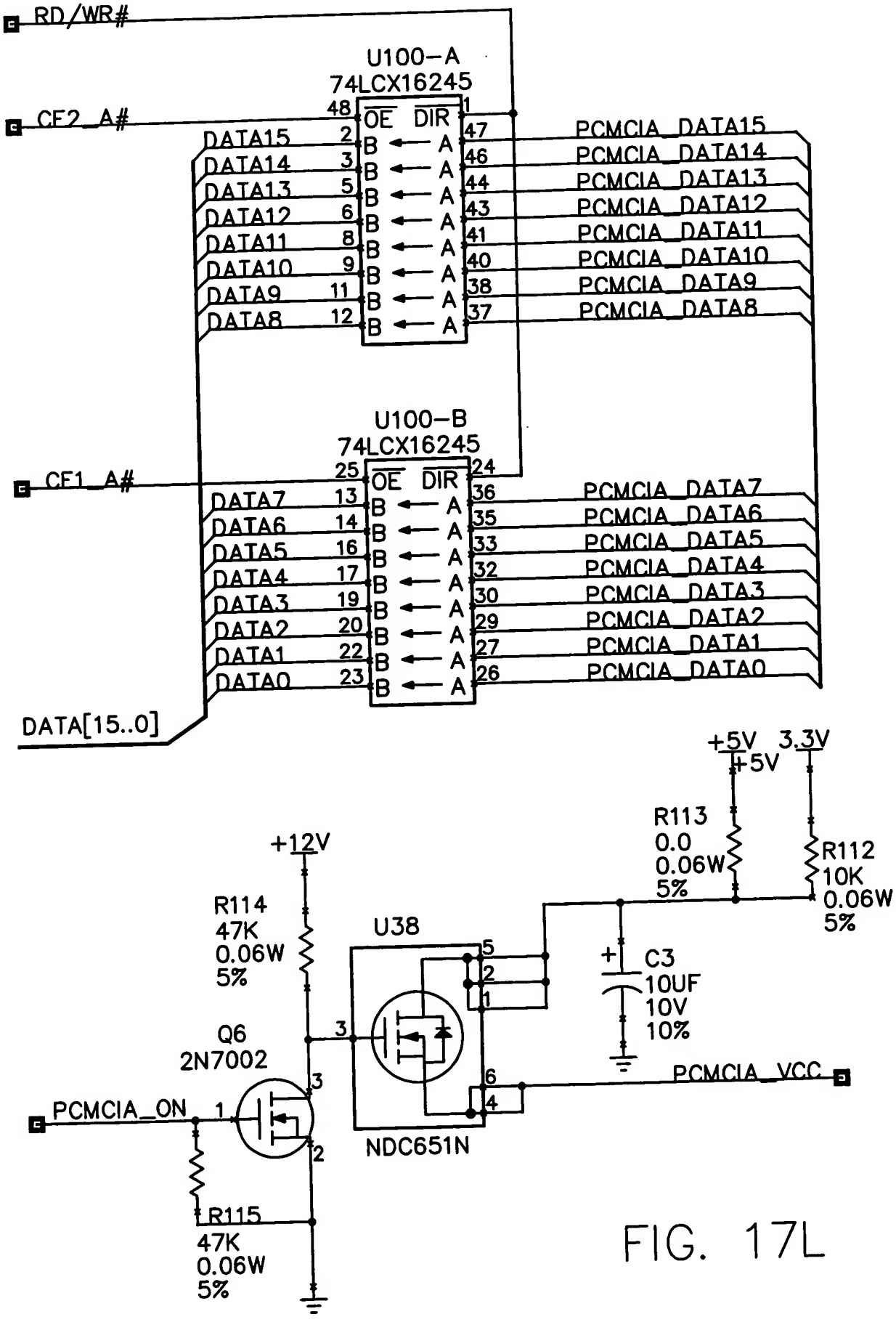
RD/WR#
U100-A
74LCX16245
CF2_A#
OE DIR
DATA15 2 B ← A 47 PCMCIA_DATA15
DATA14 3 B ← A 46 PCMCIA_DATA14
DATA13 5 B ← A 44 PCMCIA_DATA13
DATA12 6 B ← A 43 PCMCIA_DATA12
DATA11 8 B ← A 41 PCMCIA_DATA11
DATA10 9 B ← A 40 PCMCIA_DATA10
DATA9 11 B ← A 38 PCMCIA_DATA9
DATA8 12 B ← A 37 PCMCIA_DATA8
U100-B
74LCX16245
CF1_A#
OE DIR
DATA7 13 B ← A 36 PCMCIA_DATA7
DATA6 14 B ← A 35 PCMCIA_DATA6
DATA5 16 B ← A 33 PCMCIA_DATA5
DATA4 17 B ← A 32 PCMCIA_DATA4
DATA3 19 B ← A 30 PCMCIA_DATA3
DATA2 20 B ← A 29 PCMCIA_DATA2
DATA1 22 B ← A 27 PCMCIA_DATA1
DATA0 23 B ← A 26 PCMCIA_DATA0
DATA[15..0]
+5V
3.3V
+5V
R113
0.0
0.06W
5%
R112
10K
0.06W
5%
+12V
R114
47K
0.06W
5%
U38
C3
10UF
10V
10%
Q6
2N7002
PCMCIA_ON
PCMCIA_VCC
NDC651N
R115
47K
0.06W
5%

FIG. 17L

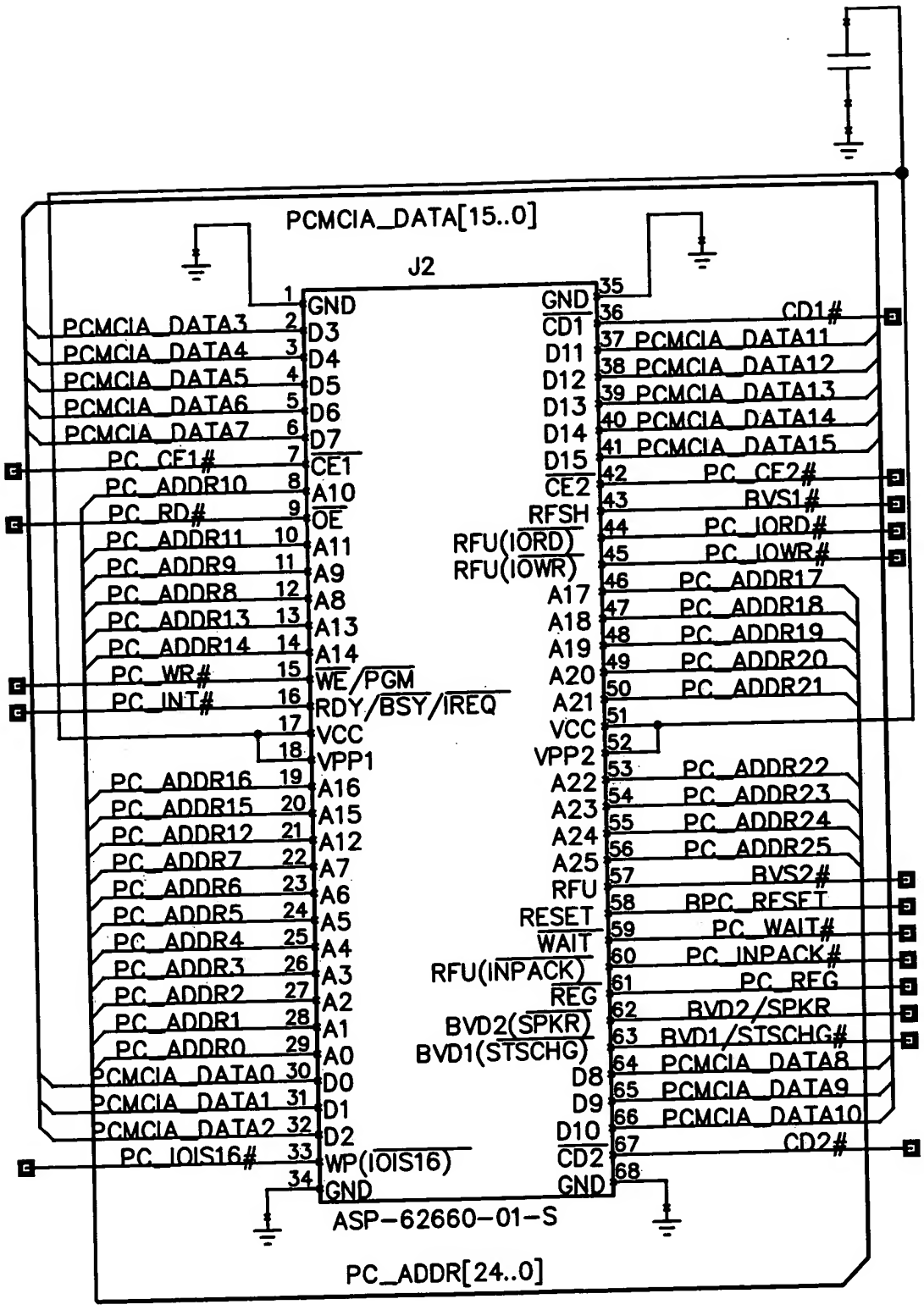
PCMCIA_DATA[15..0]
J2
1 GND
PCMCIA_DATA3 2 D3
PCMCIA_DATA4 3 D4
PCMCIA_DATA5 4 D5
PCMCIA_DATA6 5 D6
PCMCIA_DATA7 6 D7
PC_CE1# 7 CE1
PC_ADDR10 8 A10
PC_RD# 9 OE
PC_ADDR11 10 A11
PC_ADDR9 11 A9
PC_ADDR8 12 A8
PC_ADDR13 13 A13
PC_ADDR14 14 A14
PC_WR# 15 WE/PGM
PC_INT# 16 RDY/BSY/IREQ
17 VCC
18 VPP1
PC_ADDR16 19 A16
PC_ADDR15 20 A15
PC_ADDR12 21 A12
PC_ADDR7 22 A7
PC_ADDR6 23 A6
PC_ADDR5 24 A5
PC_ADDR4 25 A4
PC_ADDR3 26 A3
PC_ADDR2 27 A2
PC_ADDR1 28 A1
PC_ADDR0 29 A0
PCMCIA_DATA0 30 D0
PCMCIA_DATA1 31 D1
PCMCIA_DATA2 32 D2
PC_IOIS16# 33 WP(IOIS16)
34 GND
35 GND
36 CD1 CD1#
37 D11 PCMCIA_DATA11
38 D12 PCMCIA_DATA12
39 D13 PCMCIA_DATA13
40 D14 PCMCIA_DATA14
41 D15 PCMCIA_DATA15
42 CE2 PC_CE2#
43 RFSH RVS1#
44 RFU(IORD) PC_IORD#
45 RFU(IOWR) PC_IOWR#
46 A17 PC_ADDR17
47 A18 PC_ADDR18
48 A19 PC_ADDR19
49 A20 PC_ADDR20
50 A21 PC_ADDR21
51 VCC
52 VPP2
53 A22 PC_ADDR22
54 A23 PC_ADDR23
55 A24 PC_ADDR24
56 A25 PC_ADDR25
57 RFU RVS2#
58 RESET RPC_RESET
59 WAIT PC_WAIT#
60 RFU(INPACK) PC_INPACK#
61 REG PC_REG
62 BVD2(SPKR) BVD2/SPKR
63 BVD1(STSCHG) BVD1/STSCHG#
64 D8 PCMCIA_DATA8
65 D9 PCMCIA_DATA9
66 D10 PCMCIA_DATA10
67 CD2 CD2#
68 GND
ASP-62660-01-S
PC_ADDR[24..0]

FIG. 17M